Inkjet Printed Interconnects for Multilayer Flexible Electronics

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Abstract:

We have developed a method to fabricate fully interconnected flexible multilayer circuits at a high rate using inkjet printing. Ink containing silver nanoparticles was used for the conducting layers, and SU-8 2002 photopolymer was used for the insulating layers. During fabrication, vias with diameters between 65 μm 0and 100 μm were printed consistently, and the measured resistance of the multilayer interconnects differed little from that of single layer circuits. Bend tests revealed a slight increase in resistance, which stabilized with repeated bending.

Introduction:

Inkjet printing is emerging as an efficient and versatile method for the mass production of flexible electronic devices, such as organic light-emitting diode (OLED) displays, phased-array antennae and radio-frequency identification (RFID) tags. Many such devices require complex circuitry, which can take up considerable space. Thus, there is need for a method to create multilayer circuits in order to make the devices more efficiently utilize the available real estate.

The main objective of this project was to develop a method to reliably create multilayer interconnections for printed electronics at a high rate. The aim was to consistently create via holes that had a diameter of 100 μm or less. In addition, the process needed to be completely additive and able to be implemented using a high speed roll-to-roll printer for high throughput manufacturing.

Experimental Procedure:

The printing process involved printing a bottom conducting layer on a flexible Kapton® substrate, followed by a middle insulating layer containing via holes, and finally a top conducting layer, which connected to the bottom layer through the vias. Silver nanoparticle ink was used for the conducting layers and SU-8-2002 photopolymer was used for the insulating layer. These materials were chosen because they were readily available; however, this technique can be implemented using any printable material ink.

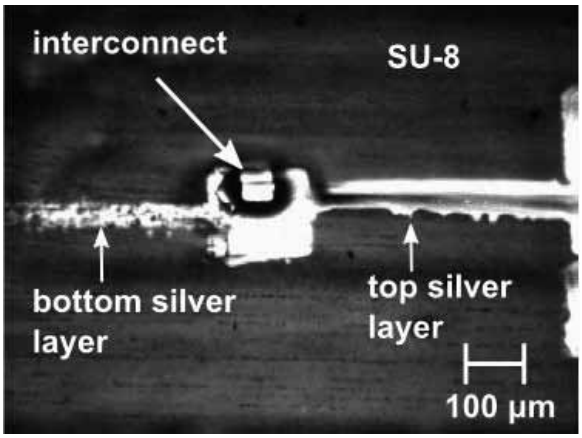
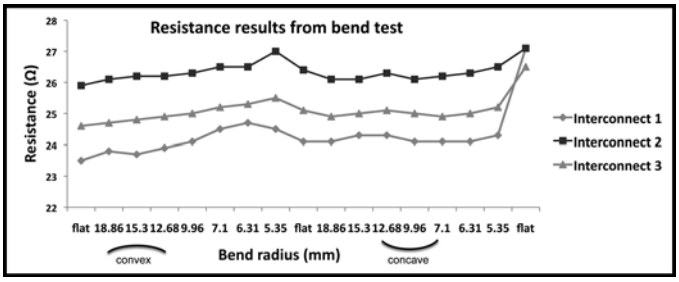


Figure 1: Optical image of multilayer interconnect.

The circuit elements were designed using AutoCAD and printed using a Fujifilm Dimatix Materials Printer, DMP 2800. The layers were aligned using ink-jet printed silver alignment marks on the flexible substrate and the printer's fiducial camera. The bottom silver layer was printed on the substrate and annealed at 150°C for permanency and conductivity. The SU-8 layer containing via holes was then printed on top of the bottom silver layer and cured using heat and ultraviolet radiation. The SU-8 was treated with oxygen plasma to increase its wettability. The entire structure was heated at 150°C to prepare the SU-8 surface for the top silver layer. The top silver layer was printed and annealed on the SU-8 with interconnects to the bottom layer through the vias (Figure 1).

In order to determine the minimum printable via hole size, we printed holes with sizes ranging from 20 μm to 180 μm using SU-8, (100 holes of each size), and determined how many were left open after printing. The minimum printable hole diameter was 120 μm in the design file, but the printed diameter was between 65 μm and 100 μm due to the viscosity of the SU-8. Ninety-nine percent of the holes of this size were open.

A test structure was printed with one via hole in the insulating layer connecting a top conductor to a bottom conductor.



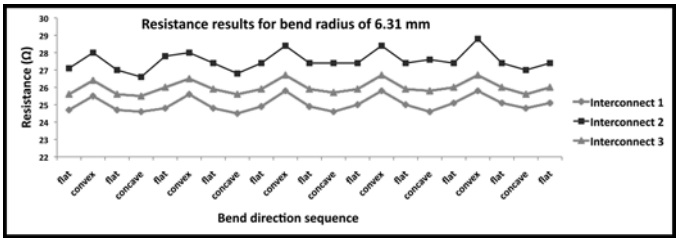


Figure 2, top: Resistance of test structure during first bend test sequence.

Figure 3, bottom: Resistance of test structure during second bend test sequence.

A digital multimeter was used to measure the resistance of the test structure. The structure was then wrapped around cylindrical rods of different radius, and a multimeter was used to measure the resistance at each bend radius.

Finally, a multilayer daisy-chain test structure was constructed to demonstrate continuity through multiple interconnects, and insulation between unconnected conductors.

Results:

The measured resistance of the test structure was 34.33 Ω. Assuming an average thickness of 0.4 μm [1] we calculated the resistivity to be 4.08×10^{-8} Ω.m and the sheet resistance to be 0.10 Ω/square. These values are both well within the range of published specifications for silver ink [1], however, they can be further improved by optimizing the annealing conditions.

Resistance of the test structure increased with decreasing convex bend radius, as expected, with slight decreases for concave bending (Figure 2). A large increase in resistance was observed in the flat state after concave bending. The increases in resistance were due to silver particles in the via being stretched apart, and the decrease in resistance for concave bending was due to the particles being compressed and forming a stronger contact [2].

An additional bend test was performed using a single bend radius of 6.31 mm in order to determine whether resistance would stabilize or continue to increase with repeated bending. Small fluctuations in resistance in the bent positions were observed, but resistance in the flat position stabilized for the last three to five measurements (Figure 3).

The daisy-chain structure successfully demonstrated continuity between interconnected conductors with acceptable resistance, and insulation between unconnected conducting layers.

Conclusions:

Our goal of developing a fully inkjet printed interconnection process for flexible electronics was successfully achieved. The via hole size was small enough to fit our constraints and the resistance of the interconnects proved to be stable with repeated bending. Unlike current interconnection methods, this process is completely additive and no chemicals are needed to remove material. This process can be implemented using a high speed roll-to-roll printer for high throughput manufacturing in the future.

Acknowledgments:

This work was funded by the National Science Foundation and the National Nanotechnology Infrastructure Network Research Experience for Undergraduates Program. The author would also like to thank Ray T. Chen, Harish Subbaraman, and Xiaohui Lin for their guidance and support.

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Investigation of Molybdenum Disulfide Transistors with Aluminum Oxide Passivation

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Abstract:

Two methods were investigated as a means of achieving conformal nucleation of aluminum oxide (Al_2O_3) on molybdenum disulfide (MoS_2). The first method consisted of depositing a thin metal layer on MoS_2, and the second method was treating the MoS_2 with oxygen (O_2) plasma. Next, four types of MoS_2 back gate transistors were fabricated and treated with a different metal layer or O_2 plasma. Electrical measurements were then compared.

Introduction:

To further Moore's law, two dimensional (2D) materials are being investigated as a possible replacement for silicon in transistors, because of their ability to achieve a thickness smaller than 1 nm. The 2D material graphene, which has been extensively investigated, does not intrinsically possess a bandgap, preventing it from being used in logic transistors; on the other hand, the 2D material MoS_2 does possess a bandgap. Although logic transistors have been fabricated using MoS_2 [1], there has been difficulty in obtaining a uniform deposition of the dielectric Al_2O_3 on MoS_2, as shown in Figure 1. The difficulty has been attributed to the lack of dangling bonds on MoS_2. Several treatments have been suggested to improve nucleation by intentionally producing nucleation sites on MoS_2 [2, 3]. We examine two of these methods. First is the deposition of a thin layer of metal, referred to as a seed layer. And second is an oxygen plasma treatment.

The purpose of our investigation was to find a method that would enable the production of a high quality top gate dielectric that would not degrade the performance of the device. In this investigation, we fabricated back gate transistors. Once a suitable method is determined, fabrication of top gate MoS_2 transistors with Al_2O_3 passivation will be pursued.

Experiment:

The MoS_2 flakes were obtained using micromechanical exfoliation and transferred to an Si wafer with 280 nm of SiO_2. The wafer was then split into four pieces. Three of the samples each had a different seed layer of aluminum (Al), chromium (Cr), or titanium (Ti); all were deposited by electron beam physical vapor deposition (EBPVD), with an average thickness of 1 nm. For the oxygen plasma treatment, a wafer with MoS_2 was placed in a reactive ion etcher (RIE) for 30 s, at room temperature, with a power of 55 W and a flow rate of 19 sccm. Using atomic layer deposition (ALD), 25 nm of Al_2O_3 was deposited on all four samples at 200°C. Inspection was done using an atomic force microscope (AFM). As shown in the AFM image in Figure 2, all four treatments did achieve conformal nucleation of Al_2O_3 on the MoS_2 flakes.

Figure 1: Al_2O_3 deposition on MoS_2 flakes with no treatment. The black regions are devoid of Al_2O_3.

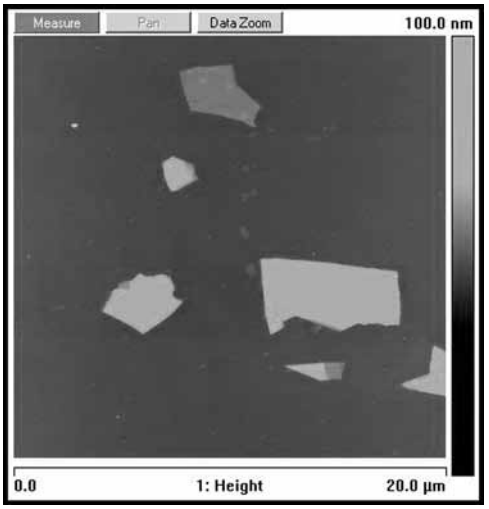

Figure 2: Uniform deposition of Al_2O_3 on MoS_2 flakes with Al seed layer. All treated samples produced similar results.

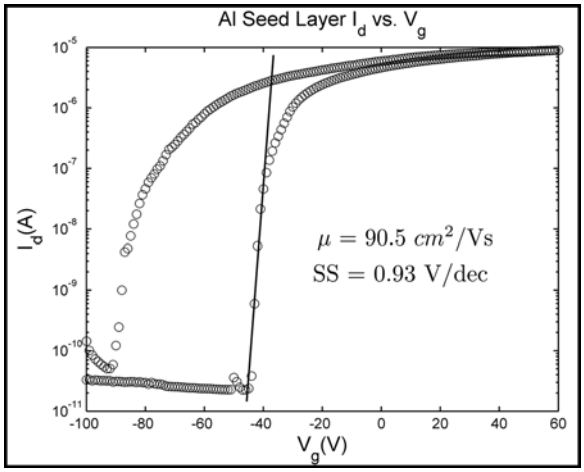

Figure 3: I_d vs. V_g hysteresis of Al seed layer transistor.

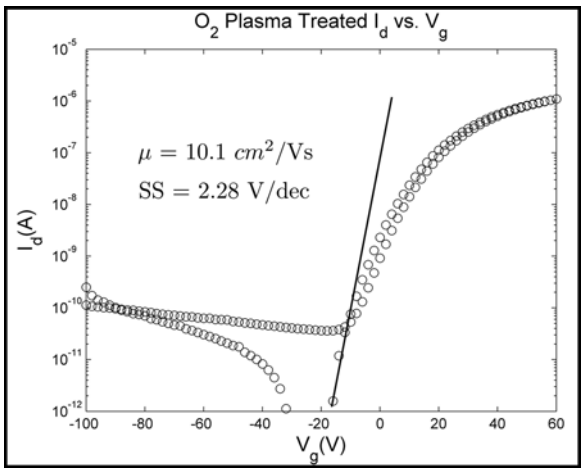

Figure 4: I_d vs. V_g hysteresis of O_2 treated transistor.

For the fabrication of the back gate transistors, four wafer samples with MoS_2 flakes had two layers of resist spin-coated onto the substrate, with MMA on the top and PMMA on the bottom. Next, the metal contacts were fabricated employing electron beam lithography for the pattern, followed by the deposition of 50 nm of gold using EBPVD, and finally lift-off. Then, each of the four samples received a different treatment, just as the four samples mentioned above. Three had a different seed layer; the thicknesses were 8Å for Al and 6Å for both Cr and Ti. The fourth sample was treated with O_2 plasma. Lastly, Al_2O_3 was deposited. The electrical measurements were collected using a two point probe, where the substrate served as the bottom gate.

Results:

The electrical measurements that were collected from the transistors included mobility and the subthreshold slope. From the results, it appeared that, out of the four, the best performance came from the transistor with the Al seed layer, with a mobility of 90.5 cm^2/Vs and a subthreshold slope (SS) of 0.93 V/dec, as shown in Figure 3. The Cr seed layer transistor had a mobility of 47.9 cm^2/Vs and a SS of 3.01 V/dec. And the Ti seed layer transistor had a mobility of 38.1 cm^2/Vs and a SS of 0.99 V/dec. Finally, the oxygen plasma treated transistor had a mobility of 10.1 cm^2/Vs and a SS of 2.28 V/dec.

Although the O_2 plasma treated transistor did not have impressive numbers, its I_d vs. V_g graph was intriguing, as seen in Figure 4. The threshold voltage shifted significantly to the right and the hysteresis curve was narrower than any of that produced by the seed layer transistors. Further analysis showed that the poor measurement numbers were not entirely due to the O_2 treatment and could be mostly attributed to the MoS_2 flakes. This finding is promising for further investigations of the O_2 treated transistors.

Conclusions:

Two methods were investigated as a means of achieving conformal nucleation of Al_2O_3 on MoS_2. The first treatment was the deposition of a seed layer, and the second was an O_2 plasma treatment. From the electrical measurements, it appears that the Al seed layer transistor had the best improvement in mobility, and the O_2 treated transistor showed promise for modifying the threshold voltage and the hysteresis effect. Future work includes an investigation to see if the current results are reproducible, and further analysis will be done to determine the cause of the observed effects.

Acknowledgements:

Thank you, Dr. Akinwande, for welcoming me into your group. Thank you, Sherry, for being my mentor. And thank you to the NNIN REU Program, NASCENT, and NSF for making this opportunity possible.

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Fabrication of Accelerometers using Paper MEMS Substrates

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Abstract:

The purpose of this research project was to make an accelerometer using microelectromechanical systems (MEMS) with paper as the substrate. This method was chosen because it was inexpensive; the fabrication process was fast and did not require specialized tooling or cleanroom time. Piezoresisitive material changes resistance and or capacitance when force is applied. We designed a number of experiments to determine this relationship. Our test design consisted of paper cantilevers on which piezoresisitive carbon ink and conductive silver ink were painted. Our results indicated a linear relationship between the applied force and resistance and capacitances shown by from the respective graphs. Next we designed an accelerometer by arranging a number of cantilevers in a circular configuration with a central seismic mass. We programmed an Arduino Uno to measure the change in capacitance and correlate that to a change in voltage. The measured voltage we then converted to acceleration and the subsequent G-Force.

Introduction:

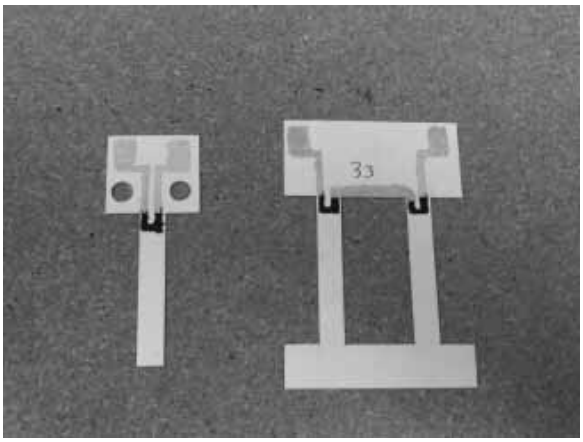
The applications and uses of microelectromechanical systems (MEMS) have grown significantly over the last decade. MEMS are microelectronic devices that can be used as sensors, actuators, and energy conversion devices and much more [1]. Our goal for the research project was to fabricate an accelerometer using paper and piezoresistive material. We observed and correlated the relationship between the applied force and change in resistance and capacitance on the piezoresistive material [2]. Using this relationship of piezoresisitive material, we designed and implemented an accelerometer for the measurement of concussive forces. By using paper as the substrate for the accelerometer, it will greatly reduce the cost of fabrication without significantly reducing the performance of the device.

Fabrication and Experimental Procedure:

We designed paper MEMS cantilevers to test and correlate the relationship between force and capacitance. We used the software Corel Draw X5 to design our cantilevers and an Epilog Helix Laser to cut out the design of the cantilevers.

Next carbon-based piezoresistive was painted on the fulcrum of the cantilever and a silver-based conductive ink for the contacts.

We used a Wheatstone bridge circuit consisting of two known resistors a potentiometer and our MEMS to measure resistance changes of the paper MEMS cantilever with applied force [3]. A micro-probe holder was used to lower the cantilever end onto the weighing balance, to determine the specific force on the cantilever. By applying a force onto the cantilever, a compressive force was transferred to the piezoresistive material causing a change in resistance. The potentiometer was adjusted until the voltage read zero. The resistance of the potentiometer was then read using a multi meter.



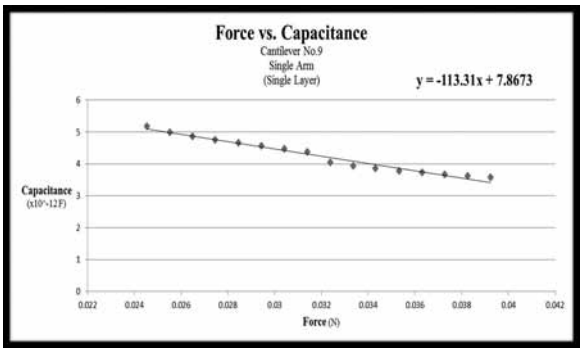


Figure 1, top: Single and double arm cantilever.

Figure 2, bottom: Force vs. capacitance single arm cantilever (single layer).

By applying an equation for the Wheatstone bridge, the unknown resistance of the cantilever was calculated and therefore correlated to the applied force.

Capacitance changes were tested using the micro-probe holder to adjust the force on the balance. A capacitance meter was used to measure the change in capacitance, which could then be converted, to a force. Experiments were made using single arm cantilevers, and double arm cantilevers, as well as single and double layers of each (Figure 1). The sensitivity of each cantilever was determined from the slope of the graphs. From our results we were able to establish a linear relationship between the applied force and the change in resistance and capacitance (Figure 2).

For the next part of our research, we designed and fabricated an accelerometer to measure concussions. The accelerometer was fabricated using four cantilevers, four springs in a circular configuration, with a seismic mass in the center. When there is an applied force the movement of the seismic mass translated the force by the cantilevers to the piezoresistive material causing a change in capacitance of the MEMS. We used an Arduino Uno to convert this capacitance change to a useable voltage from which we were able to calculate the G-Force (Figure 3). We fabricated, tested and optimized several accelerometers to increase the accuracy of the accelerometer.

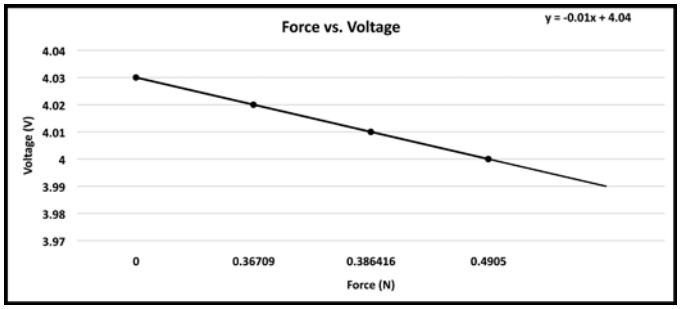


Figure 3: Applied force vs. voltage.

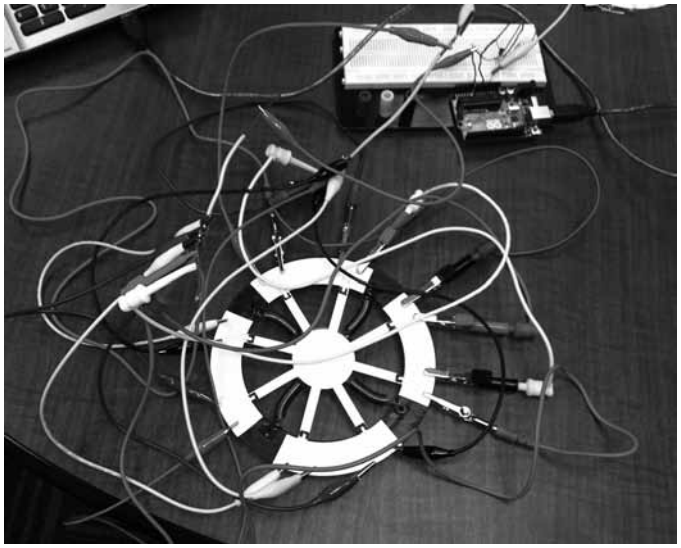


Figure 4: Accelerometer final design.

Results and Conclusions:

We successfully designed and implemented a series of experiments to establish a linear relationship between applied force and the change in resistance and capacitance of the piezoresistive carbon material. Using this relationship we designed and fabricated an accelerometer constructed from paper capable of measuring concussive forces. This fabrication was inexpensive and gave us effective results.

Acknowledgements:

I would like to thank Dr. William L. Rose, Dr. Gary L. Harris, and all the staff at Howard Nanoscale Science and Engineering Facility (HNF). I am thankful to the National Nanotechnology Infrastructure Network Research Experience for Undergraduates (NNIN REU) program, and the National Science Foundation (NSF) for giving me this great internship opportunity.

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[2] http://www.nanomotion.com/piezoelectric-effect.html
[3] http://www.engineersedge.com/instrumentation/wheat_stone_bridge.htm
[4] http://www.gracey.co.uk/downloads/accelerometers.pdf

Nanoscale High-Speed Transparent Electronics using E-Beam Patterning of Zinc Tin Oxide Thin Film Transistors

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Introduction:

Zinc tin oxide semiconductors can be used to produce transparent thin film transistors. These transistors are needed for many new applications in heads up displays and invisible microsystems. The focus of this project was to miniaturize the gate length of zinc oxide-based transistors to below 100 nanometers and characterize the performance of these transistors as a function of their gate length. As the gate length of a transistor is reduced the drive current increases, thus increasing circuit speed and performance [1].

Here, we used electron beam (e-beam) lithography to fabricate narrow gate length zinc tin oxide transistors. A beam of electrons bombards a layer of resist, creating the desired patterns. Since the size of the beam is very narrow we are able to fabricate very small features. However, when using e-beam patterning to create sub 100-nm geometries, we must take into account the proximity effect. The proximity effect involves the back-scattering of electrons once they penetrate the resist and substrate and interact with other atoms. Back-scattering of electrons causes further exposure and enlargement of the desired pattern [2].

Experimental Procedure:

First, we characterized the e-beam exposure and lift off of molybdenum (Mo) and titanium (Ti) electrodes with narrow gaps using poly(methyl methacrylate) — PMMA — resist on glass (Corning Eagle XG). Pairs of electrodes had designed gaps ranging from 10 μm to 40 nm. We exposed these structures with dosages of 600, 700, 800, 900, and 1000 microCoulombs/cm^2 using the JEOL 6300FS Electron Beam Lithography System. Lift off was then performed and the electrodes were inspected by scanning electron microscope (SEM) and electrically tested to determine whether the gap was open (as intended) or electrically shorted (indicating incomplete patterning or lift off).

The detailed process is as follows. We spun a 10 nm thick layer of PMMA A2% and soft baked for three minutes at 180°C. A 200 nm layer of e-spacer was spun on top of the resist and soft baked at 110°C for two minutes. E-spacer is a conductive polymer needed to ground the glass substrate and prevent electron deflection when using the e-beam. After e-beam lithography, the sample was dipped in distilled water for 45 seconds to strip the e-spacer, the PMMA resist was developed in 1:3 methyl isobutyl ketone : isopropyl alcohol for 30 seconds, and the sample was rinsed in isopropyl alcohol for 30 seconds. Finally, 40 nm of source/drain metal was deposited. For liftoff, the samples were left in a room-temperature acetone bath overnight, following which the bath is heated at 60°C for 1.5 hours with moderate sonication.

Once the narrow-gap electrode process was complete, we used photolithography to pattern the larger source/drain structures needed for electrical testing. E-beam lithography is a serial write process and would require a massive amount of time to write these structures. We used SPR 1813 resist and exposed using an MA/BA6 contact aligner tool. We developed the resist in MF 319; 100 nm of the secondary source/drain material was then deposited and lifted off in acetone. The electrodes were characterized using a SEM and current-voltage (I-V) measurements were taken using an Alessi probe station and HP 4155A semiconductor parameter analyzer.

For transistor processing, the samples additionally contained patterned gate metal, insulator, and patterned semiconductor layers which were prepared before the source/drain metal was deposited.

Results and Conclusions:

Figure 1 plots the measured gap between e-beam patterned electrodes as a function of the designed gap width and the e-beam dose. Gaps larger than 100 nm were not significantly affected by the differences in dosage. Using evaporated Ti, we consistently obtained separated electrodes for gaps of 40 nm and above. The electrode separation was verified by electrical testing, which indicated a very high resistance of greater than 5×10^8 Ohms, as seen in Figure 2. Electrodes with gaps down to 20 nm were fabricated using Ti (Figure 3), although their yield was not consistent. In contrast, sputtered Mo had difficulty lifting off for electrode gaps of < 500 nm. We then fabricated working transistors using photolithography to determine the effectiveness of a new separated gate and gate insulator process. Figure 4 shows electrical data for a transistor with a channel width of 100 μm and a channel length of 6 μm. The low off current and gate current, as well as the large on current indicate that the transistor is working properly.

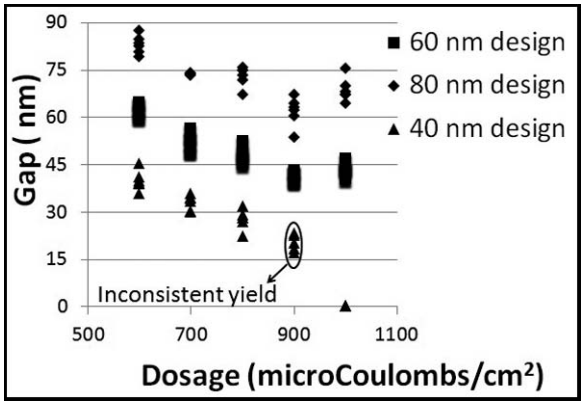

Figure 1: Electrode gap as a function of electron beam dose.

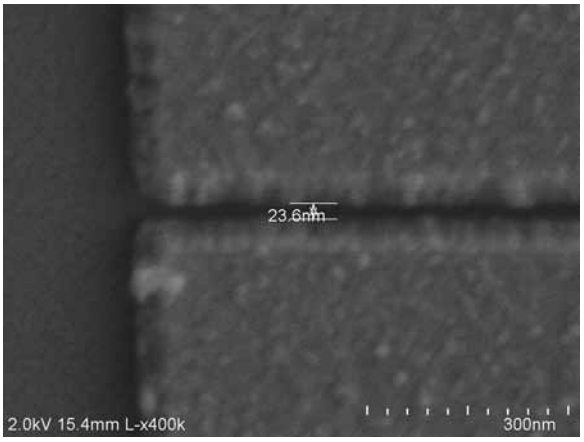

Figure 3: Open gap between 40 nm designed titanium electrodes.

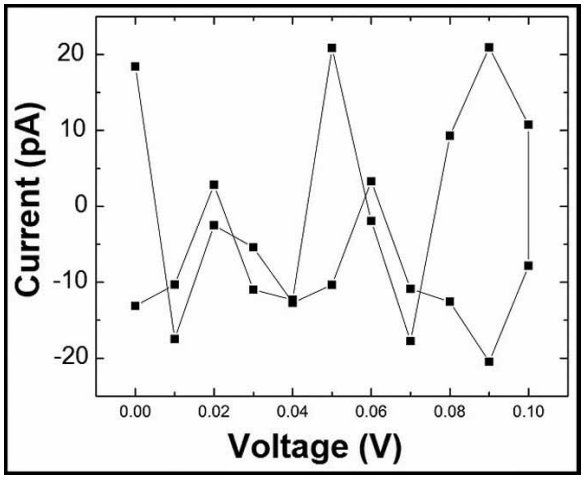

Figure 2: I-V measurement of 40 nm designed titanium electrode, indicating an open gap.

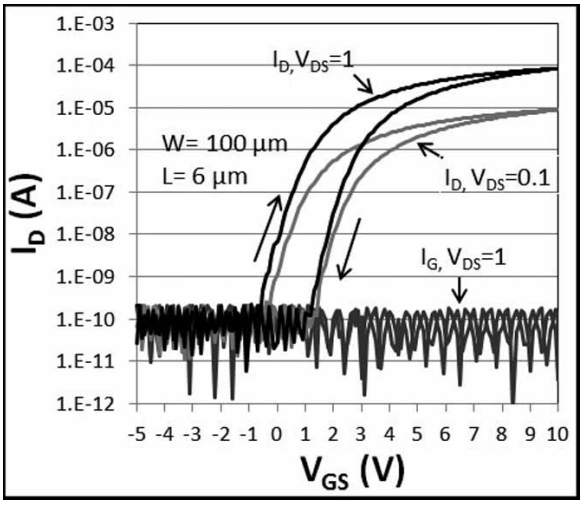

Figure 4: Electrical characteristics of photolithographically-defined transistor.

In conclusion, we were able to use e-beam lithography on transparent glass substrates to fabricate electrodes with sub 100-nm gaps. Since we were using a non-conductive substrate, a conductive polymer layer was needed to disperse charge build up. Evaporated titanium electrodes with gaps of 40 nm and above and sputtered molybdenum electrodes with gaps of 500 nm and above were consistently produced. We believe the conformality of sputtering causes difficulty for molybdenum lift off. We also were able to produce working transistors using a new separated gate and gate insulator process.

Future Work:

With successful transistors produced using photolithography, the next step is to integrate the narrow gap electrodes made using e-beam lithography into the new gate and gate insulator process to form transistors with sub-100 nm gate lengths, and then characterize their performance.

Acknowledgments:

I would like to thank my principal investigator and my mentor for their help throughout my research. I would also like to thank the Lurie Nanofabrication Facility staff, especially Dr. Vishva Ray, for their support. Finally, I would like to acknowledge financial support from the National Science Foundation for NSF BRIGE Award #ECCS1032538 and the National Nanotechnology Infrastructure Network Research Experience for Undergraduates (NNIN REU) Program.

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Zinc Oxide Based Ultraviolet Solar Cells for Self-Powered Smart Window Application

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ELEC

Abstract:

A controlled study was completed in order to determine the best structure for a zinc oxide (ZnO) based solar cell that could be used to drive an electrochromic stack. Gold (Au), aluminum (Al), silver (Ag), and the organic polymer poly(3,4-ethylenedioxythiophene) poly(styrenesulfonate), or PEDOT:PSS, were used as top contacts for the device with the aim of creating a Schottky barrier junction with ZnO. The devices were fabricated on both silicon (Si) and indium tin oxide (ITO) substrates. The most effective solar cell structure showed an open circuit voltage (V_{oc}) of 1.90 V and a short circuit current density (J_{sc}) of 0.180 μA/cm^2. However, the device had an ideality factor of 1.66 and an efficiency of 0.057%, indicating that several loss mechanisms are hindering its performance.

Introduction:

Integrating electrochromic films into existing business and residential windows has been proposed as a way of reducing building power consumption by cooling it in a passive manner. A voltage can be applied to the electrochromic stack, thereby increasing its opacity and blocking the solar infrared and ultraviolet radiation from entering the structure and heating the interior. ZnO based solar cells are promising candidates for supplying such a voltage, as ZnO possesses a wide bandgap, is visibly transparent in thin film microstructures, and forms a large Schottky barrier with a variety of metals and organic compounds, including Au (0.71 eV) [1], Ag (0.69 eV) [2], and PEDOT:PSS (0.9 eV) [3].

In theory, a device containing a ZnO-metal Schottky diode is capable of driving an electrochromic stack.

Experimental Procedure:

The solar cells to be investigated were fabricated using highly-doped Si (20 mΩ/cm) and ITO coated glass substrates that were sputtered with 1 μm of ZnO. All of the devices were then treated with an oxygen plasma for fifteen minutes to clean the surface and to increase its hydrophilic nature. PEDOT:PSS was then dynamically spun onto half of the devices at 5000 rpm for 60 s and then annealed on a hot plate in air at 160°C for five minutes. Gold and aluminum top contacts were evaporated onto all of the devices using a shadow mask. Conductive silver paint was also applied to the devices as an inexpensive alternative to evaporated silver contacts. A device schematic is shown in Figure 1.

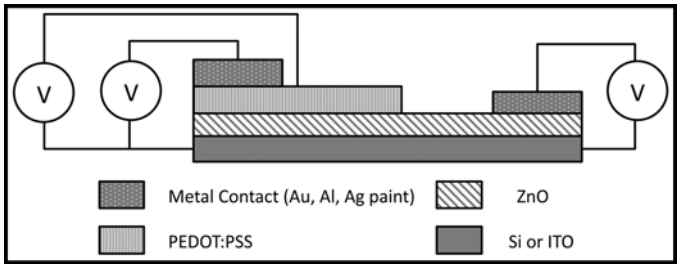

Figure 1: Schematic of a complete solar cell, showing all of the contact configurations that were used.

To characterize the performance of the solar cells, the current-voltage characteristics of each were measured under dark conditions as well as under a halogen white light lamp and a 365 nm ultraviolet lamp.

Results and Conclusions:

The current-voltage (I-V) measurements of the devices proved to be inconsistent, and not all devices exhibited a photovoltaic response. Of the devices that did show a photovoltaic response, the best performance came from one with a Au/PEDOT : PSS/ZnO/Si structure, exhibiting a V_{oc} of 1.90 V and a J_{sc} of 0.180 μA/cm^2. The I-V characteristics and dark current density plot for this device are shown in Figure 2 and Figure 3, respectively. However, the device possessed an ideality factor of 1.66 and an efficiency of just 0.057% and did not exhibit diodic behavior. The devices that did not show a photovoltaic

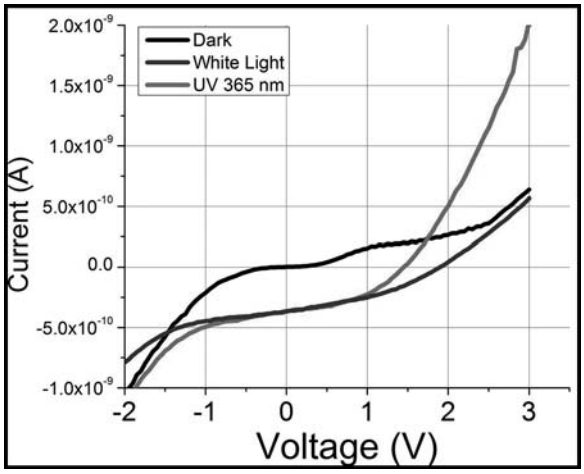

Figure 2: I-V characteristics of the Au/PEDOT:PSS/ZnO/Si device. The offset between the dark and illuminated currents indicates a photovoltaic response. However, the curve does not resemble that of a diode.

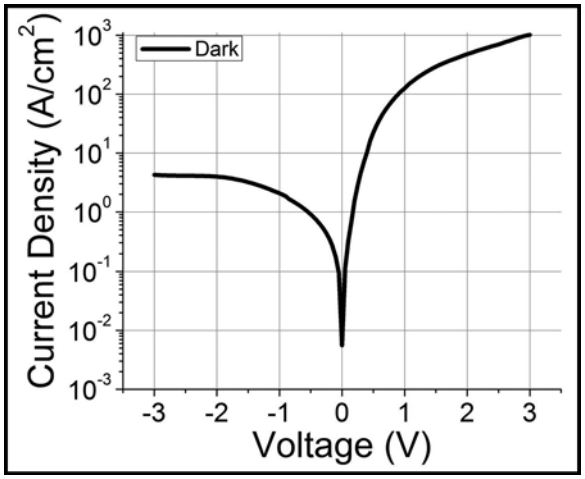

Figure 3: Dark current density plot for the Au/PEDOT:PSS/ZnO/Si device.

response demonstrated consistent rectifying behavior with Au contacts, but the Al and Ag contacts only showed occasional rectifying behavior. None of the PEDOT:PSS contacts showed rectifying behavior.

It is also of note that none of the devices that showed a photovoltaic response also showed rectifying behavior; conversely, the devices that showed rectifying behavior did not show a photovoltaic response. This is likely due to the presence of several loss mechanisms within the devices, including spontaneous polarization, oxygen deficient surfaces, grain boundaries, and recombination at the surface and back contacts. It is believed that recombination is the most significant of these mechanisms.

Future Work:

Deep-level transient spectroscopy must be used to measure the electrical defects so that they can be targeted and mitigated. If recombination is determined to be a major factor in the compromised performance in the solar cells, an electron blocking layer could be introduced to inhibit the process. The V_{oc} and J_{sc}, and efficiency of the devices could also be improved by treating the PEDOT:PSS layer so as to enhance its conductivity. Xia et al. has proposed that dilute sulfuric acid treatments of PEDOT:PSS can enhance its conductivity to ~ 3000 S/cm [4]. P-type doping of the photoactive ZnO layer could also be explored, possibly enabling the use of a p-n junction rather than a Schottky barrier junction.

Acknowledgements:

I would like to thank my Principal Investigator, Dr. Hongbin Yu, and my mentor, Ali Azhar, for all of their help and guidance. I would also like to thank the Center for Solid State Electronics Research and the Leroy Eyring Center for Solid State Science for all of the research support that they provided. Finally, I extend my gratitude to the National Nanotechnology Infrastructure Network and the National Science Foundation for their funding contributions and organization of the Research Experience for Undergraduates program.

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Researching All-Aluminum n-Type Silicon Solar Cells

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Abstract and Introduction:

One of the fundamental bottlenecks for silicon solar cells in reaching terawatt scales is the scarcity of silver (Ag). Furthermore the price of Ag has been rising sharply. We have proposed that Ag should be replaced by other metals. In order to improve these contacts, high doping level layers were fabricated on the both sides of our cells.

Generally, p-type silicon wafers are used in solar cells, but in our research n-type wafers are used. These types of solar cells have enormous potential to be high efficiency solar cells. However they have a few problems due to the surface states on the surface of the p^+-type layer. In order to increase cell performance, an aluminum oxide (Al_2O_3) layer has been chosen for a passivation layer, it is also a dielectric containing a fixed negative-charge density. This effect results in the reduction of surface recombination.

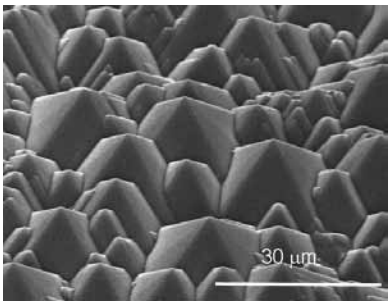

Figure 1: SEM of the surface texturing.

Experiment Procedure:

First the random texturing was fabricated on the both sides of a cell for reducing the reflectance. By using the anisotropic wet etching method, the pyramid shape texturing was fabricated.

Second, the diffusion processes were applied to the samples for fabrication of the cell structure. There were three steps in the diffusion processes. The n^+-type back surface field (BSF) layer was fabricated in the phosphorus diffusion process. This layer worked as a barrier against minority carriers in the n-region. The depth and the donor concentration of n^+-type layer were controlled by firing time and temperature. Boron diffusion was also applied to the cell in order to make a p^+-type layer after the first diffusion. Subsequently the sample was annealed at 1050°C in nitrogen ambient gas. This is called the "drive-in diffusion process." In order to reduce the doping concentration on the each surface of the cell, we applied the drive-in diffusion.

Third, the aluminum was sputter deposited on the both sides. After metallization, the Al_2O_3 was applied on the front surface as a passivation layer. Subsequently the front surface was covered with SiN_x. These SiN_x/Al_2O_3 layers worked as an anti-reflection coating. Finally, the sample was annealed in ambient forming gas ambient at 350°C.

Results:

By using anisotropic wet etching, the pyramid shape texturing was fabricated on the both sides (Figure 1). Reduction of reflectance was observed because of this texturing. Finally, after deposition of SiN_x, the average of reflectance became 4.53% in the range from 300 nm to 1000 nm.

After diffusion processes, depth dependent doping concentrations was measured (Figure 2). From this doping profile, we could observe that the doping concentrations on the both surfaces were still high. It means that the drive-in diffusion did not work.

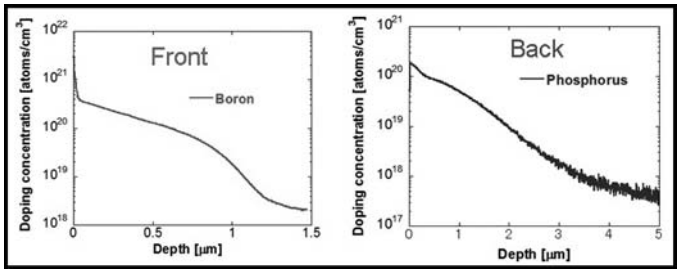

Figure 2: Depth dependent doping concentrations on the both sides.

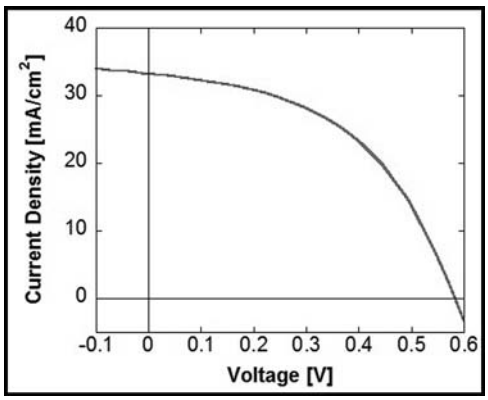

Figure 3: I-V characteristic.

After finishing all processes, all samples showed short-circuited behavior. In order to remove some parts which were short-circuited, the samples were cut into some pieces. After cutting the samples, the I-V characteristic measurement was taken (Figure 3). The surface area was 5 cm^2 and 20% of it was covered with front electrode. From this assumption, each parameter was calculated. The efficiency achieved was 9.3%.

The doping profile indicates the drive-in diffusion did not work. We assume that after the diffusion for fabrication of the p^+-layer, boron silicate glass (BSG) was formed on the surface and then during the drive-in diffusion, the boron diffused into the samples from the BSG. Because of it, the high doping concentrations on the surface were formed and some parts of the samples were short-circuited.

Each parameter was compared with some references [1, 2]. From this comparison and I-V characteristics, low fill factor showed us that there was large leakage current and series resistance (Figure 4). This series resistance included the problems of contacts however we could not investigate them separately. Low open-circuit voltage (V_{oc}) and short-circuit current density (J_{sc}) were mainly because of high recombination rate. From the doping profile, high doping concentrations on the surface and deeper junction helped recombination occur at high rates on the front surface.

Conclusions and Future Works:

In conclusion, an all-aluminum n-type Si solar cell was fabricated. The efficiency achieved was 9.3%. Random texturing was fabricated to reduce the reflectance. From J_{sc} and V_{oc}, high surface recombination was identified for the low efficiency. From the doping profile, the high doping concentrations on the surface reduce diffusion lengths and deeper junction allows recombination near the front surface.

For next steps, we should apply an *in situ* oxidation step in order to remove the BSG after the diffusion process for the p^+-layer. This process is supposed to make it possible to fabricate the samples which have the desired doping profile and do not need to cut into some pieces. Form this effect, the larger surface area of the samples improves the fill factor by reducing the leakage current and series resistance, whereas lower doping concentrations on the front surface help to reduce recombination near the front surface.

Acknowledgments:

I would like to thank my PI, Prof. Meng Tao, and my mentor Wen-cheng Sun for all of their help and guidance. Thanks also to the National Nanotechnology Infrastructure Network International Research Experience for Graduates (NNIN iREG) Program, the National Science Foundation, the Nanotechnology Platform Japan, and the Center for Solid State Electronics Research at Arizona State University for research support and funding.

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	J_{sc} [mA/cm^2]	V_{oc} [mV]	FF	η [%]
Our Sample	33	590	0.48	9.3
From Some References	40	700	0.80	23

Figure 4: Comparison each sample parameters with other studies.

Trap Density Analysis of High Dielectric Oxides on III-V Semiconductors

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Abstract and Introduction:

The prospect of III-V semiconductors offer a higher efficiency alternative to the commonly used silicon, which is currently facing size limitations. One of the major problems surrounding the III-V semiconductors is the high trap density (D_{it}) between the oxide and semiconductor interfaces. In this project, metal-oxide-semiconductor capacitors (MOSCAPs) were fabricated using different annealing processes and time frames. Three experiments were conducted on the MOSCAPS for midgap D_{it} analysis. First, three samples were annealed using forming gas, nitrogen (N), and oxygen (O), respectively. Next, three samples were annealed to 300, 350, and 400°C. Finally, a sample which underwent metal deposition one week after being annealed was compared with a sample with no such time delay. Capacitance-voltage (CV) and conductance-voltage (GV) data was extracted from each sample using the impedance analyzer and manipulated to reveal information about the midgap D_{it}.

Experimental Procedure:

The MOSCAP samples were fabricated in several steps. Initially, an $In_{53}Ga_{47}As$ substrate was doped with silicon and wet cleaned. The sample was put in the atomic layer deposition (ALD) reactor at 300°C, where it was cleaned for nine cycles with N_2 plasma/TMA, followed by oxide deposition of 35 cycles HfO_2 to the top surface. The sample was then annealed to various temperatures in different gasses. Using the thermal evaporator, Ni was deposited to the top of the sample while Cr and Au were deposited to the bottom.

Both the conductance and Terman methods were used for data analysis, and there are several differences between the two. The conductance method uses only raw data, while the Terman method uses raw and ideal data. The conductance method is most useful at low frequencies (1 kHz), while the Terman method is most useful at high frequencies (1 MHz). Finally, the conductance method shows only the midgap D_{it}, which is around 0.3 eV, while the Terman method shows a broader range for the trap density.

In this research, however, the Terman method showed results that were either negligible or contradictory to the conductance method, which was considered more reliable since it uses only the raw data. We think this could either have been because of impurities across the interfaces of the samples or because the non-midgap D_{it} among samples was too close to analyze. For this reason, this paper will only discuss results from the conductance method.

In the first part of the project, we compared samples that were annealed in different gases: forming gas (95% nitrogen, 5% hydrogen), nitrogen and oxygen. Figure 1 shows the raw CV data for the different samples at 1 kHz frequency.

The area of most interest was the midgap bump in the negative bias region. A smaller bump would indicate a lower midgap D_{it}. Figure 1 shows a lower bump for the oxygen-annealed sample, which would indicate that oxygen is a better annealing gas than forming gas and nitrogen.

Another way to interpret this data is with a G_p/w 3D plot. Shown in Figure 2, G_p/w is a function of capacitance, conductance, and the natural properties of the sample at every voltage and frequency point. This is useful because the midgap D_{it} is roughly 2.5 times the peak of this graph. Figure 2 shows the G_p/w data for the oxygen annealed sample.

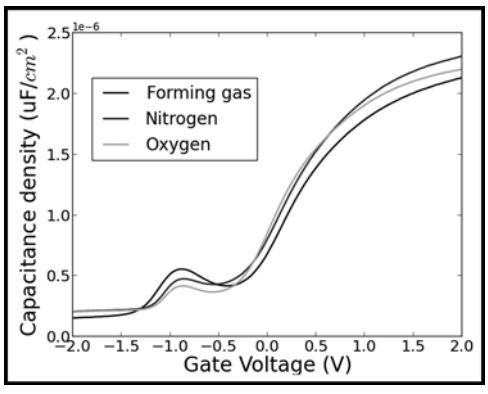

Figure 1: CV curves for samples annealed in different gases.

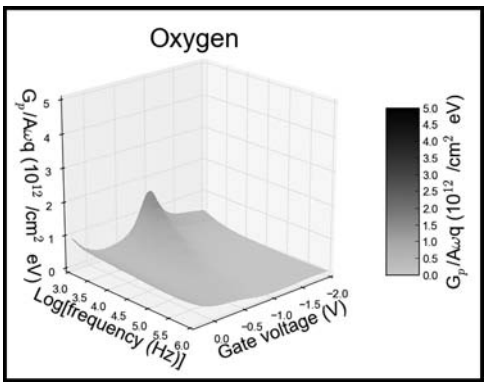

Figure 2: 3D G_p/w plot for samples annealed in different gases.

While the graphs for the other samples are not shown, the peak for the oxygen annealed sample was in fact lower, which shows that oxygen was in fact a better annealing gas.

In the next part of the project, we varied the annealing temperature, while keeping a constant ramp rate. Figure 3 shows the CV data for the three samples, which were annealed to 300, 350, and 400°C. It is apparent from Figure 3 that the optimal annealing temperature was 400°C. We could see, however, that there was a very small difference between 350 and 400°C, while the sample annealed at 300°C was significantly worse. This led us to believe that since the sample was put in the ALD at 300°C, it was important to anneal it to a higher temperature than that.

In the final part of the project, we compared two samples with the same fabrication parameters, but one sample underwent metal deposition a week after it has been annealed, while in the other metal was deposited on the same day. Figure 4 shows the CV curves for these two samples. There was a vast difference between the two, as it was clear that the smaller bump belongs to the sample that was metal-deposited on the same day. This experiment was important to run because if this discovery hadn't been made, it could have tarnished our other comparisons.

In this project, we noticed a lower midgap D_{it} in the samples that were annealed in oxygen at high temperatures with gate metal deposited immediately after annealing. We concluded that these were favorable conditions for lowering the trap density in HfO_2/n-InGaAs MOSCAPS.

There are still many more parameters to test and a great deal more work to be done to achieve a low enough trap density, but our discoveries are a step in the right direction for determining the optimal fabrication process for these devices.

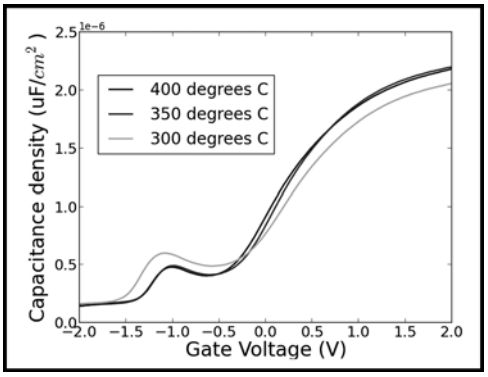

Figure 3: CV curves for samples annealed to different temperatures.

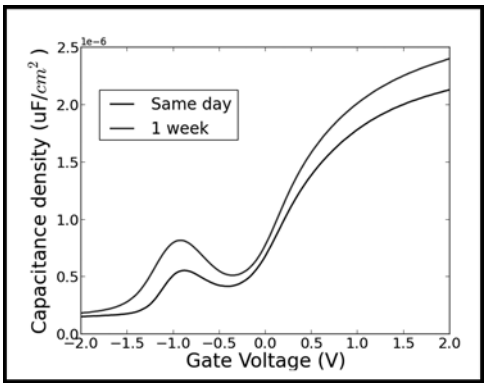

Figure 4: CV curves for samples with different time conditions.

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Influence of Planar Organic Electrochemical Transistor Device Geometry in the Characterization of Barrier Tissue

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Introduction:

The interfacing of electronics with biological systems, using novel organic materials that are easily processed, have soft mechanical properties, and the ability to conduct both ions and electrons, has led to endless applications in the field of bioelectronics. Organic electrochemical transistors (OECTs) are one application of this innovative technology [1].

Our aim for this project was to take various geometric aspects of the OECT, diagramed in Figure 1, and evaluate the effects the variable had on the electrical characteristics of the transistor and in the characterization of barrier tissue. Planar OECTs offer the advantages of a simple fabrication process — cells can be seeded directly on top of the transistor and the electrical and optical characterization can be correlated since the device is fully transparent. The p-type semiconductor poly(3,4-ethylened ioxythiophene):poly(styrenesulfonate) (PEDOT:PSS) was used as the active layer for the gate and the channel. The contacts were made of gold [2]. When a positive voltage was applied to the gate, the cations, from the cell media, were pushed into the PEDOT:PSS channel layer. The film was thus dedoped, becoming less conducting.

Madin-Darby canine kidney (MDCK) epithelial cells were grown on top of the transistors imitating barrier tissue, which regulates the passage of ions, nutrients, and pathogens through both transcellular and paracellular transportations. Barrier tissue integrity was electronically measured by the OECT and the optimal device geometry was determined.

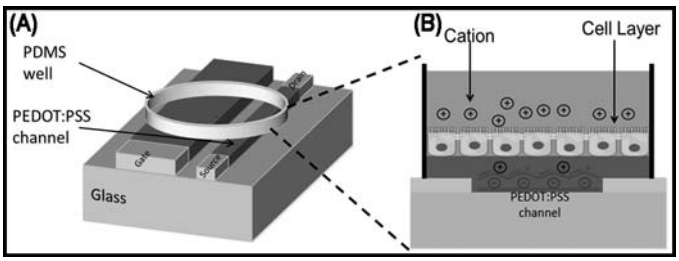

Figure 1: (A) Schematic of the planar OECT with PEDOT:PSS gate and channel on the same plan. (B) Cross section of the OECT sensor with cells grown on it. The presence of this cell layer modulates the flux of ions that can penetrate in the PEDOT:PSS channel.

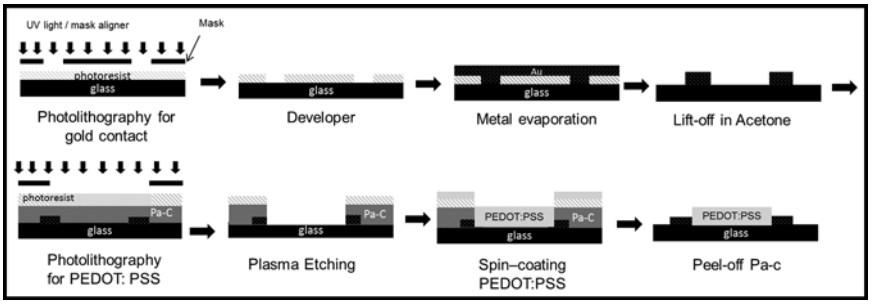

Figure 2: Organic electrochemical transistor fabrication process.

Device Fabrication:

For the fabrication of planar OECT, shown in Figure 2, glass substrates (75 mm × 25 mm) were obtained, cleaned, spin-coated with S1813 photoresist, and patterned with the desired device geometry using photolithography. The substrates were developed in MF-26 developer. Using the metal evaporator, 10 nm of chromium and 100 nm of gold, was deposited on the surface. Acetone and sonication was used to remove the photoresist and excess gold, leaving patterned substrates. A 2 μm layer of Parylene C was deposited. Then AZ-9260 photoresist was spin-coated. The substrates were again exposed to UV-Light for PEDOT:PSS patterning. With the plasma etcher, areas without photoresist were removed. PEDOT:PSS was deposited on the substrates with the spin coater and the Parylene C layer was then peeled off, removing photoresist and PEDOT:PSS that was not attached to the glass substrate. The substrates were hard baked for 30 minutes at 140°C and PDMS wells where attached to each pixel on the transistor.

Characterization of OECT:

For the electrical characterization of the OECT, a probe station and a Keithley 2612 Source Meter were used. The channel current modulation under a pulsed gate was measured and the highest modulation was expected.

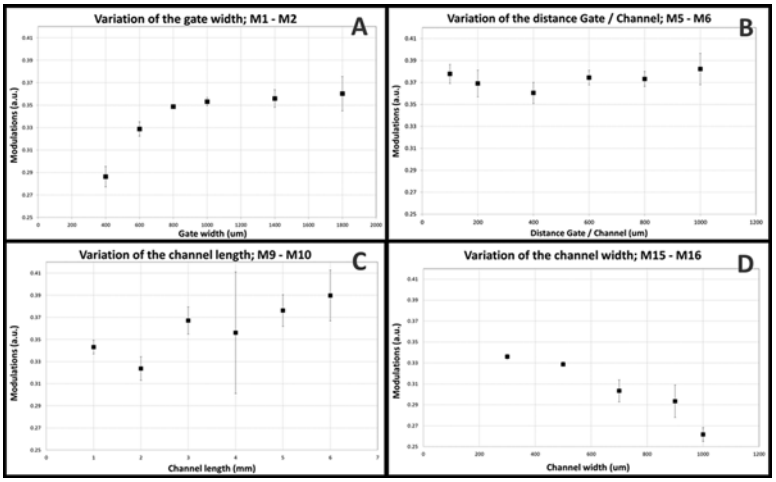

Figure 3: OECT electrical characterization, showing average and standard deviation of the modulation. A) Gate width variance (400-1800 µm), B) Distance between gate and channel variance (100-1000 µm), C) Channel length variance (1-6 mm), and D) Channel width variance (100-1000 µm).

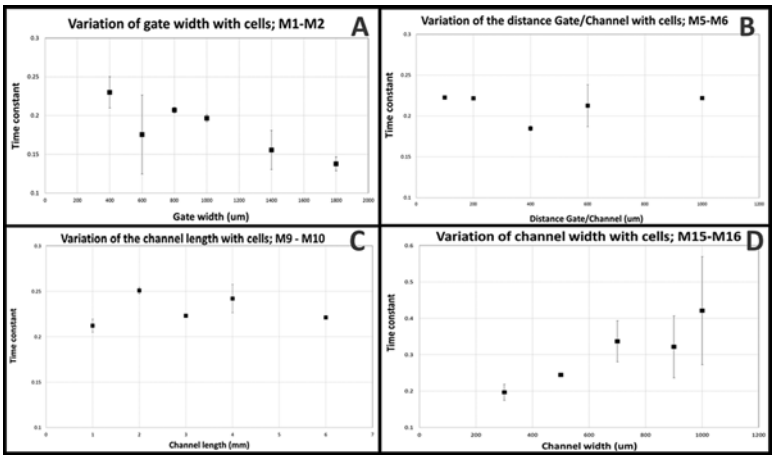

Figure 4: Characterization of barrier tissue. Average and standard deviation of Tau value are shown. A) Gate width variance (400-1800 µm), B) Distance between gate and channel variance (100-1000 µm), C) Channel length variance (1-6 mm), and D) Channel width variance (100-1000 µm).

Data for each varying parameter was obtained, the modulation graphed and standard deviation calculated (Figure 3). The same procedure was used for the characterization of the barrier tissue of MDCK cells at Day 6, according to OECT geometry. With MDCK cells, instead of modulation, the time constant Tau was used as a figure of merit representing the speed of the dedoping / doping of the channel layer. The highest Tau was expected and the data obtained was graphed in Figure 4 along with the standard deviation.

Results and Conclusions:

Varying geometric aspects of the OECT were evaluated, and the effects the variable had on the electrical characteristics of the transistor barrier tissue were observed. It was found that, initially, transistors without the layer of cells required a minimum gate width of 800 μm to dedope the PEDOT:PSS in the channel effectively (Figure 3A). From the graph of modulation versus the varying the distance between the gate and channel, in Figure 3B, it was concluded that this parameter had no effect on the success of the transistor. With an increase in channel length, an increasing trend was observed indicating that more charges were involved (Figure 3C). Increasing the channel width reduced the modulation because the ratio of the gate to channel did not remain consistent and there were not enough ions to fully dedope the channel.

In the presence of a cell layer, increasing gate width reduced the Tau value (Figure 4A) indicating that a larger gate was required in order to push ions through the cell barrier. Variation of the distance between the channel and gate and of the channel length did not have an effect on the Tau value (Figure 4B and 4C). Increasing the channel width improved the Tau value (Figure 4D) leading to the conclusion that with a larger channel covered with cells, it takes longer for the ions to be passed through the cell barrier.

Overall it can be concluded that in both sets of data, channel and gate width have a large and opposite effect on the OECT biosensor illustrating the importance of the (gate / channel) aspect ratio. An aspect ratio (area gate / area channel) of 8 is a good tradeoff between high enough modulation and Tau value, effectively dedoping the PEDOT:PSS while still monitoring small changes in the barrier tissue integrity. The distance between the gate and the channel does not affect the modulation or the time constant. When increasing the channel length, the modulation increases without increasing the Tau value, because there is an increase in the number of charges. The fact that the Tau value stays constant demonstrates the independence of the sensibility (represented by Tau) to the length and by extension to the area of the OECT.

Acknowledgments:

I would like to thank Professors George Malliaras and Roisin Owens, the Bioelectronics Laboratory, and Dr. Marc Ramuz for their guidance. I am grateful to the NNIN iREU Program and NSF for this research opportunity.

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Examining Metal/SnS Contact Resistances for the Increase of SnS Solar Cell Efficiency

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Abstract:

Many current solar cell technologies use toxic elements (such as cadmium) and rare elements (such as tellurium, indium, and gallium) in their construction. These components add expense and are major impediments to increased usage of solar cell technologies. As a result, research is being done into solar cells that use non-toxic and abundant elements such as tin (II) sulfide solar cells. The focus of this research was the investigation of the contact resistance of the metal back contact of a tin sulphide (SnS) solar cell. SnS solar cells have a record efficiency of only 2.04. This efficiency needs to be increased for these cells to be commercially viable.

Background:

Tin (II) sulfide solar cells utilize SnS deposited onto a metal back contact via atomic layer deposition (ALD). The production and structure of these cells is described by Sinsermsuksakul et al. [1]. A crucial part of a solar cell is the metal back contact (molybdenum in the case of Sinsermsuksakul [1]). This contact between SnS and the metal contributes a resistance to the electrical circuit known as the contact resistance. This contact resistance affects the efficiency and by selecting a contact with a low contact resistance, the overall efficiency of the cell should be increased.

The method used to examine the contact resistance of the metal/SnS contact is known as the transmission line method (TLM). Specifically, the method used was the transmission line method with circular patterns, similar to the method described by Deepak [2]. This method involves measuring the resistance of metal patterns on a substrate and using the physical geometry of the patterns to determine both the contact resistance of the metal and the sheet resistance of the substrate.

This research involved examining patterns of different metals to determine their contact resistances with SnS. The metals examined were aluminum, gold, copper, indium, molybdenum, nickel, and titanium.

Experimental Procedure:

First, samples of SnS were formed by depositing SnS onto thermal oxide on silicon via atomic layer deposition (ALD). All of the samples were as deposited by the ALD reactor and some were then annealed in H_2S. The samples next had the circular metal patterns deposited onto them. The metal patterns were created by using photolithography to create a pattern of exposed substrate and then depositing 300 nm of the metal onto the sample with electron beam evaporation. After this process, the remaining mask pattern was removed, leaving just the circular metal patterns on the surface.

After the metal patterns were created on the SnS substrates, the resistance of each pattern was determined via I-V probe testing. This testing revealed that copper, indium, and aluminum created non-Ohmic contacts and thus did not need to be investigated further as they would not lead to an increase in efficiency. However, nickel (Ni), titanium (Ti), molybdenum (Mo), and gold (Au) did form Ohmic contacts. A plot showing the current-voltage characteristic of nickel on annealed SnS is shown in Figure 1. Each line is a different pattern size. For each metal, the resistance of each pattern size was plotted against a parameter based on the geometry of the pattern. An example of this relationship for Ni on annealed SnS is shown in Figure 2. The equation of the line of best fit of these points allows values for the contact resistance and sheet resistance to be obtained. The slope is the sheet resistance and the intercept is a factor based on both the sheet resistance and contact resistance. The results of the calculations of both sheet and contact resistance for all Ohmic metals are shown in Table 1.

Results and Conclusions:

As can be seen in Table 1, gold has the lowest contact resistance. However, the cost of gold means that it could be uneconomical to use it in a solar cell that is meant to be cheaper than current technologies. Even though the identity of the substrate (either annealed or as-deposited SnS) is in question for the gold contacts, it is clear that it has the lowest contact resistance by

far. The next best choice for back contact is the currently used material, molybdenum. This means that molybdenum is still the best choice for back contact in a SnS solar cell.

As can also be seen, there was great variation in the measurements of sheet resistance for each of the samples. This was likely due to difficulties in the delicate processes involved in both fabrication and characterization. The sheet resistance values should be more consistent as the SnS films were all deposited in the same run and should thus have very similar hole concentrations and resistivities. This consistency in sheet resistance was shown in previous work by this research group. Additionally, the sample of Ni deposited onto as-deposited SnS has a rather high contact resistance in comparison to other values. This could also be due to problems in fabrication and characterization.

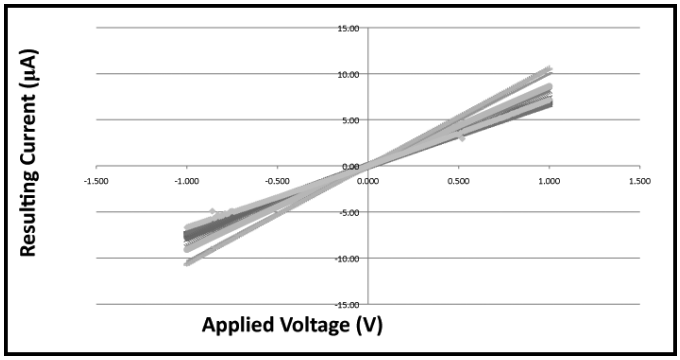

Figure 1: Current vs. voltage measurements for nickel patterns of various sizes on annealed nickel.

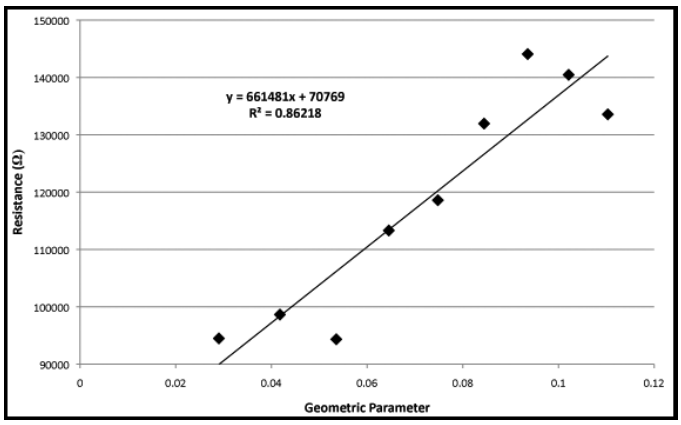

Figure 2: Resistance values of various pattern sizes vs. a geometric parameter of the pattern size. The slope of the line of best fit is the sheet resistance and the intercept is a result of the sheet resistance and the contact resistance.

Acknowledgements:

I would like to thank Professor Roy Gordon, Leizhi Sun, the Harvard Center for Nanoscale Systems, and the other members of the Gordon group for making this research possible. I would also like to thank Dr. Kathryn Hollar, the National Science Foundation, and the National Nanotechnology Infrastructure Network Research Experience for Undergrads Program for making this research opportunity possible.

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	Sheet Resistance (kΩ/sq)	Error in Sheet Resistance (kΩ)	Contact Resistance (Ω-cm2)	Error in Contact Resistance (Ω-cm2)
Annealed Nickel	661.5	100	1.868	0.496
As-Deposited Nickel	1861.3	907.4	35.588	20.092
Annealed Titanium	1424.7	94	0.662	0.154
As-Deposited Titanium	4461.3	275.2	0.343	0.194
Annealed Molybdenum	1473.5	109.6	0.163	0.085
As-Deposited Molybdenum	7232.8	123.3	0.187	0.046
As-Deposited* Gold	1858.9	70.5	0.000749	0.003582

**Gold could be on annealed SnS*

Table 1: Sheet resistance and contact resistance values for various metal patterns deposited onto both annealed and as-deposited SnS.

Radio Frequency Switches Using Phase Change Materials

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Abstract:

Phase change (PC) materials have two separate states: crystalline state and amorphous state. In the crystalline state, the electrical resistance is relatively low, while a high resistance level is observed in the amorphous state. If the two states are properly controlled and resistance level difference is sufficient throughout radio frequency (RF) range, this material can be utilized as an ohmic switch. The main goal of this project was to fabricate RF switches using germanium telluride (GeTe), a PC material. More practical structure was proposed with separate RF and heater electrodes. For better performance and effective phase transition, fabrication process was characterized. First, to improve metal contact resistance, oxidized molybdenum (Mo) electrodes in contact area with GeTe were etched using diluted hydrofluoric acid (HF) solution. Also, additional aluminum nitride (AlN) layer was deposited under the GeTe switch for better heat dissipation into the high resistivity silicon (Si) substrate. An additional oxide layer was also deposited on the bottom heater electrode to get better access to the GeTe area for phase transition and improved crystallization condition.

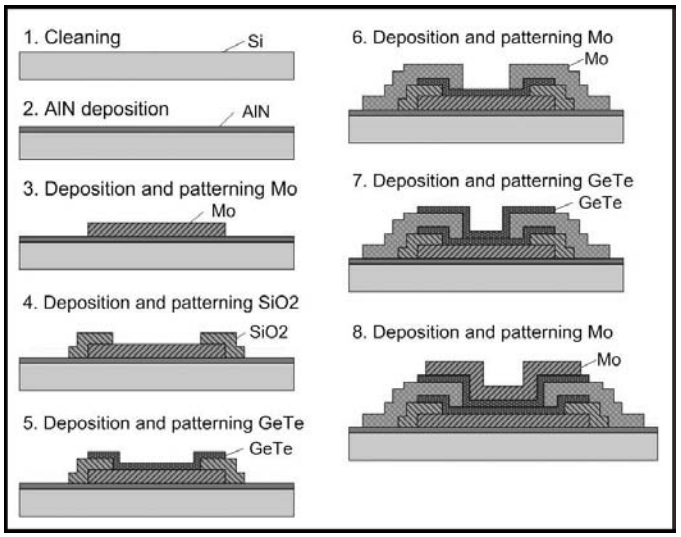

Figure 1: Fabrication flow of RF switches using phase change material.

Introduction:

These days, RF switches are used for switching signals or antennas such as wireless local area network (LAN) in mobiles phones or laptops etc. Using the RF switches, we can enable high speed communications. There are many kinds of RF switches: solid state devices, micro-electro-mechanical system (MEMS) switches and phase change switches. The most conventional ones are solid state devices. In solid state devices, electrical circuits are used for switching. MEMS switches are investigated these days and switch mechanically. Compared to solid state devices, MEMS switches have some advantages: higher linearity and lower power consumption [1, 2]. Phase change switches use PC material for switching. Compared to MEMS switches, PC switches have some advantages; having smaller size, easier integration with CMOS, lower gate voltages, and not having special packaging requirements [3].

PC materials have two separate states; crystalline state and amorphous state. In the crystalline state, the electrical resistance is relatively low, while in the amorphous state, the resistance is high. If the two states are controlled, this material can be an ohmic switch. The main goal of this project was to fabricate practical RF switches using GeTe.

Experimental Procedure:

The RF switches using PC material were fabricated on Si wafers. The fabrication flow was shown in Figure 1. Fabrication process is described below. First of all, an AlN layer was deposited on a prepared Si wafer. AlN has high insulation and high thermal conductivity so heat can easily dissipate. Next,

Mo was deposited on the AlN layer and patterned using liftoff process. This Mo layer would be the bottom heater electrode. Next, a silicon dioxide (SiO_2) layer was deposited and patterned using radical ion etching (RIE). This SiO_2 was used to insulate completely between the bottom heater electrode and the RF electrode, which would be deposited later.

The next step was depositing a GeTe layer and patterning it with liftoff process. After depositing GeTe, Mo layer was deposited and patterned using liftoff process and this layer would be the RF electrodes. Next, a second GeTe layer was deposited and patterned using liftoff process. Finally, a Mo layer was deposited and patterned using liftoff process. This Mo layer would be the top heater electrode. Right before each Mo deposition, oxidized Mo on the surface of Mo was etched using diluted HF solution, so that the electrical resistance would be lower.

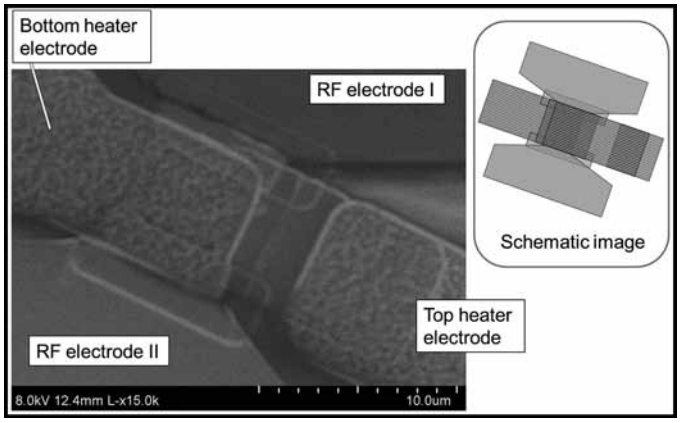

Figure 2: SEM image of structure of a phase change switch.

Results and Conclusions:

With above processes, the structure was fabricated. A scanning electron microscope (SEM) image of this structure is shown in Figure 2. Compared to the schematic image, this structure seemed to be fabricated well. Next, these devices were measured to determine if they worked or not. Voltage pulses were applied between two metals, but the phase change didn't happen. The phase change material GeTe was probably damaged.

There are many possible reasons why the GeTe was damaged: resist remover, ultrasonic cleaning, heating, diluted HF, or ashing.

Future Work:

It is important to determine which process damaged the GeTe. The GeTe should be measured at each step of the process to see if it works.

Acknowledgments:

I really would like to appreciate the following people and institutions: Prof. Mina Rais-Zadeh, Dr. Yonghun Shim, Resonant MEMS Group, Brandon Lucas, and LNF staff for their assistance; the National Nanotechnology Infrastructure Network International Research Program together with Nanotechnology Platform, Japan, and the National Science Foundation for funding.

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Fabrication and Characterization of InGaAs Metal-Oxide-Semiconductor Capacitors (MOSCaps) with HfO_2 Dielectrics

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ELEC

Abstract and Introduction:

III-V indium gallium arsenide (InGaAs) metal-oxide-semiconductor field effect transistors (MOSFETs) are promising candidates for next-generation low power logic technology. A major challenge for III-V MOSFETs is the development of suitable gate dielectrics with low interface trap densities (D_{it}). This project focused on the fabrication of InGaAs metal-oxide-semiconductor capacitors (MOSCaps) with hafnium oxide (HfO_2) dielectrics grown by atomic layer deposition (ALD). Several studies were conducted involving *in situ* ALD surface cleaning, HfO_2 growth temperature, and post-deposition forming gas anneal (FGA) parameters. The two types of surface cleaning investigated to reduce interface trap density were hydrogen (H_2) plasma/trimethylaluminum (TMA) and nitrogen (N_2) plasma/TMA. Various HfO_2 deposition temperatures were explored to probe the ALD window of HfO_2 growth. Finally, the post-deposition FGA was optimized by testing different ramp rates and annealing temperatures. The InGaAs MOSCaps were characterized using capacitance-voltage (C-V) measurements, and the interface trap densities were evaluated using the conductance method.

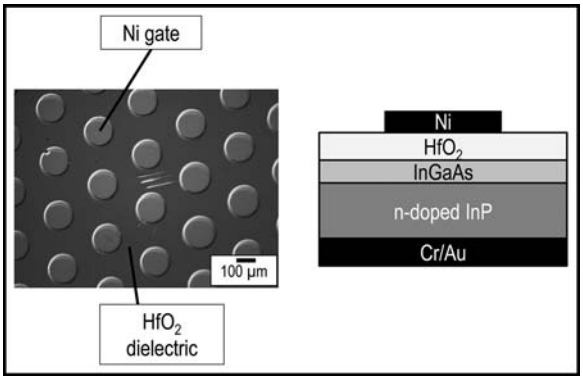

Figure 1: Top-down view of MOSCaps taken with an optical microscope (left); schematic of MOSCap from side view (right).

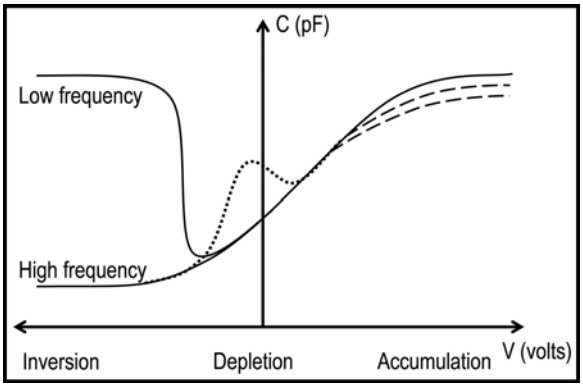

Figure 2: Ideal C-V curves shown with solid lines; mid-gap bump shown with dotted line; frequency dispersion represented with dashed lines.

Methods:

InGaAs MOSCaps were desirable for study in this project because of their short fabrication time. First, the semiconductor bulk and channel (InP/InGaAs) were grown by molecular beam epitaxy (MBE). The sample was then solvent-cleaned with acetone and isopropyl alcohol and dipped in buffered hydrofluoric acid to prepare the semiconductor surface for the oxide layer.

Before HfO_2 was deposited via ALD, the sample was again cleaned *in situ* with either H_2 plasma/TMA or N_2 plasma/TMA. The H_2 plasma/TMA and N_2 plasma/TMA were performed for five and nine cycles, respectively, as these numbers have been shown to be optimal [1]. HfO_2 was grown with a general recipe calling for a one second tetrakis(ethylmethylamino)hafnium (TEMAH) pulse and 0.5 second water pulse at 300°C, though this parameter space was explored. An oxide thickness between 40-50 Å was sought; this was accomplished by using between 35-40 cycles of TEMAH/water pulses and purges.

After ALD, the sample was annealed in forming gas. The standard conditions were 15 minutes at 400°C with a ramp rate of 75°C/min, but these parameters were also altered and studied. Upon removal from the FGA furnace, the nickel (Ni) gate and chromium/gold (Cr/Au) backside metal contacts were thermally evaporated to complete the MOSCap fabrication (see Figure 1).

Characterization of the MOSCap was completed using an impedance analyzer to extract C-V and conductance-voltage (G-V) data. C-V curves were plotted and significant attention

was paid to the size of the mid-gap bump (see Figure 2) as this was indicative of the D_{it}, with a smaller mid-gap bump signifying a smaller D_{it}.

$$G_p = \frac{\omega^2 C_{ox}^2 G_m}{G_m^2 + \omega^2 (C_{ox} - C_m)^2}$$

$$D_{it} \approx \frac{2.5}{Aq} \left(\frac{G_p}{\omega}\right)_{max}$$

Figure 3: Conductance method equations used to find D_{it}.

Frequency dispersion in the positive bias was also noted, because smaller dispersion suggested a smaller number of border traps, another oxide defect.

Furthermore, C-V and G-V data was used to quantify the D_{it} using the conductance method (see Figure 3) and assess MOSCap quality. In the conductance method, G_m and C_m are measured conductance and capacitance values, C_{ox} is oxide capacitance, ω is the frequency, G_p is the parallel conductance, A is the capacitor area and q is the elementary charge.

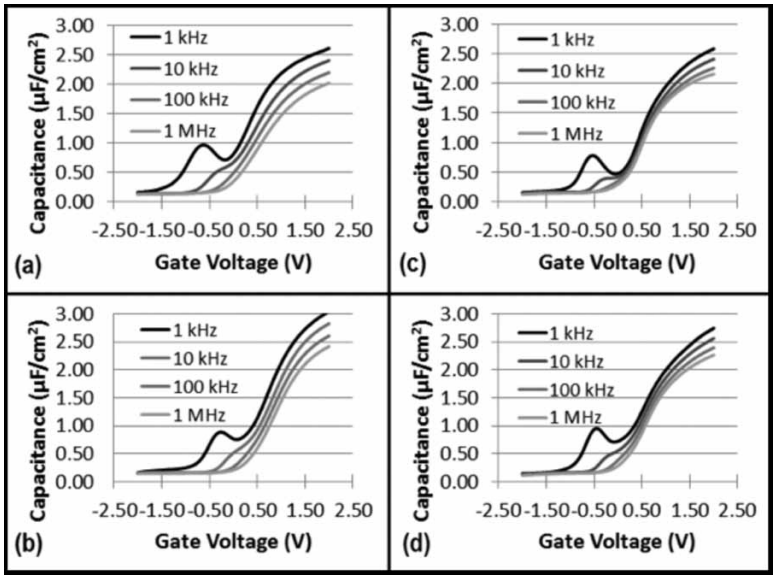

Figure 4: C-V characteristics as a function of frequency. Plots (a), (b) and (c), (d) were from samples pre-treated with H_2 plasma/TMA and N_2 plasma/TMA, respectively. Plots (a), (c) and (b), (d) were from samples subjected to FGA ramp rate of 10°C/min and 75°C/min, respectively.

Results and Conclusions:

The various studies intended to lower D_{it} and achieve good C-V profiles yielded interesting findings. Varying the ALD growth temperature of HfO_2 from 200-300°C did not substantially affect the D_{it}, though the 300°C sample did show a slightly smaller D_{it} than the others. Another study that looked at several FGA temperatures for H_2 plasma/TMA pre-treated samples confirmed, by comparing D_{it}, that 400°C was the optimal for use during annealing.

The differences in the H_2 plasma/TMA and N_2 plasma/TMA *in situ* surface cleanings did not at first appear to be noteworthy with standard growth and FGA conditions applied. Upon more closely studying the FGA parameters, an exciting observation was made. A smaller ramp rate (10°C/min) paired with N_2 plasma/TMA pre-treatment returned MOSCaps with better C-V profiles than those that coupled a higher ramp rate with N_2 plasma/TMA pre-treatment. The exact opposite was true for the MOSCaps pre-treated with H_2 plasma/TMA, which showed higher ramp rates (75°C/min) giving better C-V profiles (see Figure 4).

These results implied that *in situ* ALD surface cleaning and FGA parameters cannot be viewed entirely separately, but rather they should be taken into consideration together when trying to lower D_{it}.

Future Work:

With the discovery that *in situ* ALD surface cleaning and FGA parameters should be examined together in order to lower D_{it} in InGaAs MOSCaps, more studies will be completed that optimize the two pre-treatment methods with their respective FGA conditions. In the same vein, it should be shown why lower ramp rates during annealing reduce the D_{it} in the N_2 plasma/TMA pre-treatment devices, but higher ramp rates reduce the D_{it} in the H_2 plasma/TMA pre-treatment devices. This will be accomplished by probing the interfacial layer that develops during ALD between the oxide and semiconductor and inspecting how this layer is dissimilar depending on the surface cleaning employed.

Acknowledgments:

This project would not have been possible without the support of many parties. Many thanks are owed — the National Nanotechnology Infrastructure Network Research Experience for Undergraduates (NNIN REU) Program and National Science Foundation, for funding; Samantha Cruz, Jamie Pillsbury and UCSB Nanotech staff, for assistance; Rodwell group members, for advising; my Nanofam, for unmatched friendship and kindness. In particular, I would like to thank my mentor, Cheng-Ying Huang, for providing me with the perfect balance of encouragement and freedom for a successful summer.

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