TiO_2-Based Core/Shell Nanowires for Adding Gas Sensing Capabilities to Silicon CMOS Circuitry

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Abstract:

Silicon/titanium dioxide (Si/TiO_2) core/shell nanowires were prepared by atomic layer deposition (ALD) of a TiO_2 shell on the surface of high-aspect-ratio Si nanowires that were obtained by deep reactive ion etching (DRIE) of a high resistivity Si substrate patterned using colloidal lithography. The microstructure of the TiO_2 was determined by transmission electron microscopy (TEM) technique. In the as-deposited sample, the shell of the nanowire was found to be amorphous TiO_2. After annealing in O_2 gas at 873 K for two hours, the amorphous phase transformed into a crystalline phase, identified as anatase TiO_2. As a result, it was found that the amorphous shell transformed into anatase TiO_2 by the annealing.

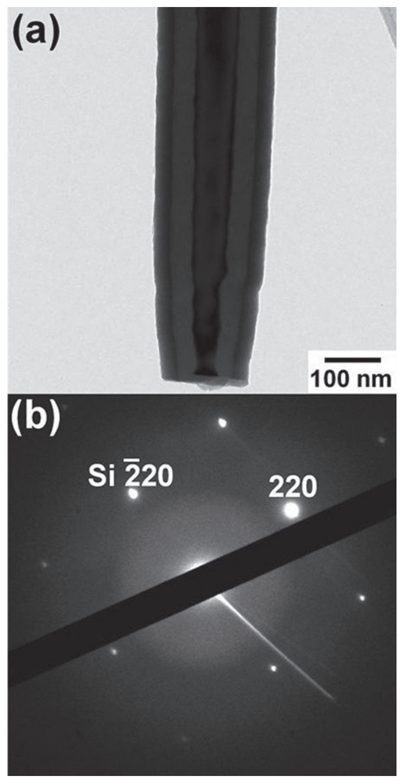

Figure 1: TEM observation of the nanowire before annealing.

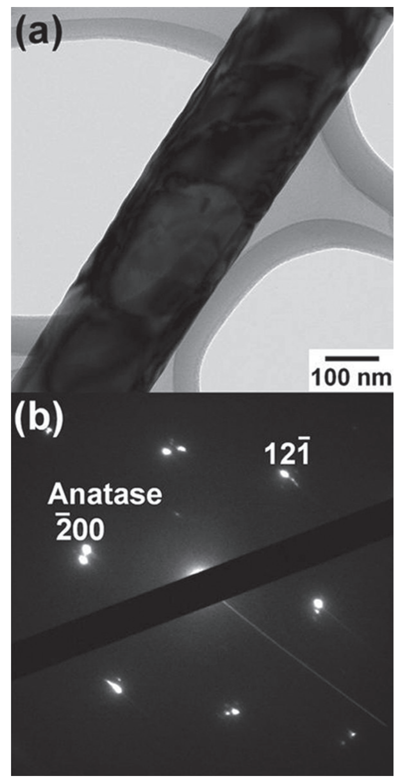

Figure 2: TEM observation of the nanowire after annealing at 873 K.

Introduction:

Electronic devices such as microprocessors, microcontrollers, static random-access memories, and other digital logic circuits are based on the complementary metal oxide semiconductor (CMOS) technology because of its low static power consumption and noise immunity. New functionalities obtained by integrating unconventional materials and devices with the Si circuitry will dramatically expand its capabilities and performance. For example, metal oxide materials designed to produce a large electronic response to chemical vapors offer sensing capabilities. However, the high temperatures required to fabricate high-sensitivity metal oxide nanowire sensors would damage the CMOS circuitry, which has made it difficult to effectively couple them in a single integrated circuit (IC) platform. Bottom-up synthesis of nanowires, composed of a diverse range of elemental or compound materials, offers a promising way to add sensing functions CMOS circuits. We have focused on using electric-field directed self-assembly to position arrays of individual nanowires synthesized using bottom-up methods at predefined locations on a CMOS substrate [1, 2].

In this project, Si nanowires coated by TiO_2 (Si/TiO_2 core/shell) were fabricated for gas sensor arrays on Si CMOS. The gas sensor performance of the wires is strongly dependent on the TiO_2 microstructural properties, including uniformity, thickness, composition, and atomic configuration [3]. The goal of this project was to clarify the relationship between the gas sensitivity and the TiO_2 microstructure. In the present study, the microstructure of different types of TiO_2-coated Si nanowires was investigated by TEM to understand the effect of thermal annealing on TiO_2 microstructure.

Experimental Procedure:

The nanowires were prepared by ALD of a TiO_2 shell on the surface of high-aspect-ratio Si nanowires that were obtained by deep reactive ion etching (DRIE) of a high resistivity Si substrate patterned using colloidal lithography. Thermal annealing was carried out at 873 K in O_2 gas for 7.2×10^3 s with a heating rate of 8.3×10^{-3} K s^{-1}. Then the substrate was allowed to cool to room temperature. The nanowires before and after the annealing were observed by TEM, capturing bright-field (BF) images and selected area diffraction (SAD) patterns.

Results:

Figure 1 shows the microstructure of the nanowire before annealing. In the BF image (a), it was found that the core of nanowire was surrounded by two shells whose contrasts are featureless. The length of the nanowire, diameter of the core and thickness of the inner and outer shells were about 5 μm, 80 nm, 40 nm and 30 nm, respectively. In the SAD pattern (b), a spot pattern and diffuse scattering disk pattern were detected. This spot pattern corresponds to that of crystalline Si <001>. The disk pattern can be attributed to the overlapping halo rings and background of the transmitted wave. These results indicate that the core was single-crystal Si and the shells were amorphous phases of the constituent materials. Further investigation is necessary to identify the exact composition of the amorphous shells; however, based on the nanowire fabrication process, the inner and outer amorphous shells are expected to be SiO_2 and TiO_2, respectively.

Figure 2 shows the microstructure of the nanowire after annealing at 873 K in O_2 gas. In the BF image (a), some grain-boundary and bend-contour contrast were observed, indicating the outer shell consists of coarse crystalline grains. All diffraction spots in the SAD pattern (b) could be indexed by anatase TiO_2 <012> diffraction spots. As a result, it was found that the outer amorphous shell transformed into coarse grains of anatase TiO_2 by annealing at 873 K. It should be noted that no significant changes in the core and the inner shell were detected following thermal annealing.

Conclusions and Future Work:

In this project, Si/TiO_2 core/shell nanowires were fabricated for gas sensor arrays. The nanowires were investigated by TEM focusing on the effect of annealing on the TiO_2 microstructure. As a result, the following conclusions were obtained:

(1) The fabricated nanowires before annealing consisted of three parts, namely, single-crystal silicon core, inner and outer amorphous shells.

(2) The outer amorphous shell transformed into coarse grains of anatase TiO_2 by annealing at 873 K.

In the future, these fabricated nanowires will be integrated onto lithographically patterned Si substrates using electric-field directed self-assembly and their gas sensitivity will be measured to clarify influence of TiO_2 microstructure.

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References:

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