Fabrication and Characterization of InGaAs Metal-Oxide-Semiconductor Capacitors (MOSCaps) with HfO_2 Dielectrics

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Abstract and Introduction:

III-V indium gallium arsenide (InGaAs) metal-oxide-semiconductor field effect transistors (MOSFETs) are promising candidates for next-generation low power logic technology. A major challenge for III-V MOSFETs is the development of suitable gate dielectrics with low interface trap densities (D_{it}). This project focused on the fabrication of InGaAs metal-oxide-semiconductor capacitors (MOSCaps) with hafnium oxide (HfO_2) dielectrics grown by atomic layer deposition (ALD). Several studies were conducted involving *in situ* ALD surface cleaning, HfO_2 growth temperature, and post-deposition forming gas anneal (FGA) parameters. The two types of surface cleaning investigated to reduce interface trap density were hydrogen (H_2) plasma/trimethylaluminum (TMA) and nitrogen (N_2) plasma/TMA. Various HfO_2 deposition temperatures were explored to probe the ALD window of HfO_2 growth. Finally, the post-deposition FGA was optimized by testing different ramp rates and annealing temperatures. The InGaAs MOSCaps were characterized using capacitance-voltage (C-V) measurements, and the interface trap densities were evaluated using the conductance method.

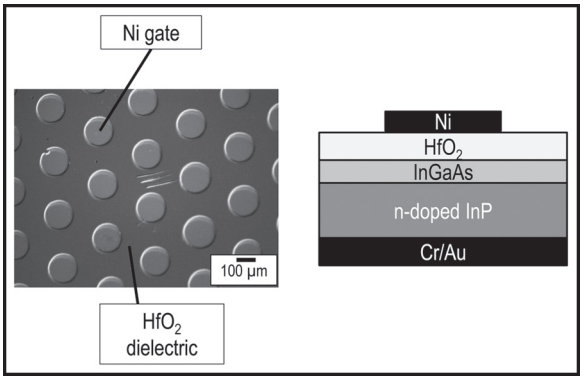

Figure 1: Top-down view of MOSCaps taken with an optical microscope (left); schematic of MOSCap from side view (right).

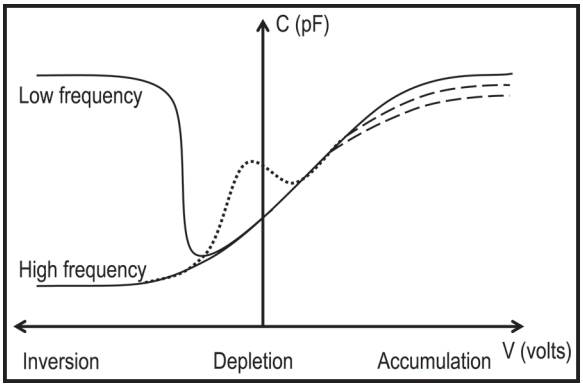

Figure 2: Ideal C-V curves shown with solid lines; mid-gap bump shown with dotted line; frequency dispersion represented with dashed lines.

Methods:

InGaAs MOSCaps were desirable for study in this project because of their short fabrication time. First, the semiconductor bulk and channel (InP/InGaAs) were grown by molecular beam epitaxy (MBE). The sample was then solvent-cleaned with acetone and isopropyl alcohol and dipped in buffered hydrofluoric acid to prepare the semiconductor surface for the oxide layer.

Before HfO_2 was deposited via ALD, the sample was again cleaned *in situ* with either H_2 plasma/TMA or N_2 plasma/TMA. The H_2 plasma/TMA and N_2 plasma/TMA were performed for five and nine cycles, respectively, as these numbers have been shown to be optimal [1]. HfO_2 was grown with a general recipe calling for a one second tetrakis(ethylmethylamino)hafnium (TEMAH) pulse and 0.5 second water pulse at 300°C, though this parameter space was explored. An oxide thickness between 40-50 Å was sought; this was accomplished by using between 35-40 cycles of TEMAH/water pulses and purges.

After ALD, the sample was annealed in forming gas. The standard conditions were 15 minutes at 400°C with a ramp rate of 75°C/min, but these parameters were also altered and studied. Upon removal from the FGA furnace, the nickel (Ni) gate and chromium/gold (Cr/Au) backside metal contacts were thermally evaporated to complete the MOSCap fabrication (see Figure 1).

Characterization of the MOSCap was completed using an impedance analyzer to extract C-V and conductance-voltage (G-V) data. C-V curves were plotted and significant attention

was paid to the size of the mid-gap bump (see Figure 2) as this was indicative of the D_{it}, with a smaller mid-gap bump signifying a smaller D_{it}.

$$G_p = \frac{\omega^2 C_{ox}^2 G_m}{G_m^2 + \omega^2 (C_{ox} - C_m)^2}$$

$$D_{it} \approx \frac{2.5}{Aq} \left(\frac{G_p}{\omega}\right)_{max}$$

Figure 3: Conductance method equations used to find D_{it}.

Frequency dispersion in the positive bias was also noted, because smaller dispersion suggested a smaller number of border traps, another oxide defect.

Furthermore, C-V and G-V data was used to quantify the D_{it} using the conductance method (see Figure 3) and assess MOSCap quality. In the conductance method, G_m and C_m are measured conductance and capacitance values, C_{ox} is oxide capacitance, ω is the frequency, G_p is the parallel conductance, A is the capacitor area and q is the elementary charge.

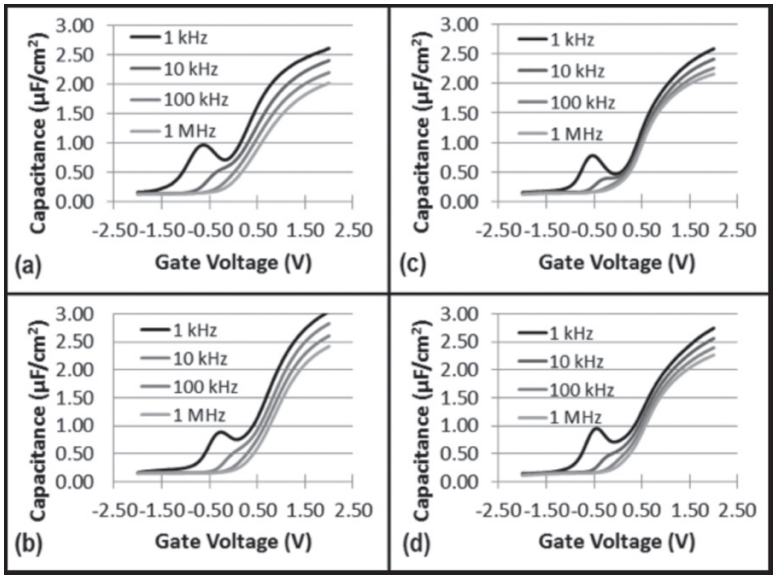

Figure 4: C-V characteristics as a function of frequency. Plots (a), (b) and (c), (d) were from samples pre-treated with H_2 plasma/TMA and N_2 plasma/TMA, respectively. Plots (a), (c) and (b), (d) were from samples subjected to FGA ramp rate of 10°C/min and 75°C/min, respectively.

Results and Conclusions:

The various studies intended to lower D_{it} and achieve good C-V profiles yielded interesting findings. Varying the ALD growth temperature of HfO_2 from 200-300°C did not substantially affect the D_{it}, though the 300°C sample did show a slightly smaller D_{it} than the others. Another study that looked at several FGA temperatures for H_2 plasma/TMA pre-treated samples confirmed, by comparing D_{it}, that 400°C was the optimal for use during annealing.

The differences in the H_2 plasma/TMA and N_2 plasma/TMA *in situ* surface cleanings did not at first appear to be noteworthy with standard growth and FGA conditions applied. Upon more closely studying the FGA parameters, an exciting observation was made. A smaller ramp rate (10°C/min) paired with N_2 plasma/TMA pre-treatment returned MOSCaps with better C-V profiles than those that coupled a higher ramp rate with N_2 plasma/TMA pre-treatment. The exact opposite was true for the MOSCaps pre-treated with H_2 plasma/TMA, which showed higher ramp rates (75°C/min) giving better C-V profiles (see Figure 4).

These results implied that *in situ* ALD surface cleaning and FGA parameters cannot be viewed entirely separately, but rather they should be taken into consideration together when trying to lower D_{it}.

Future Work:

With the discovery that *in situ* ALD surface cleaning and FGA parameters should be examined together in order to lower D_{it} in InGaAs MOSCaps, more studies will be completed that optimize the two pre-treatment methods with their respective FGA conditions. In the same vein, it should be shown why lower ramp rates during annealing reduce the D_{it} in the N_2 plasma/TMA pre-treatment devices, but higher ramp rates reduce the D_{it} in the H_2 plasma/TMA pre-treatment devices. This will be accomplished by probing the interfacial layer that develops during ALD between the oxide and semiconductor and inspecting how this layer is dissimilar depending on the surface cleaning employed.

Acknowledgments:

This project would not have been possible without the support of many parties. Many thanks are owed — the National Nanotechnology Infrastructure Network Research Experience for Undergraduates (NNIN REU) Program and National Science Foundation, for funding; Samantha Cruz, Jamie Pillsbury and UCSB Nanotech staff, for assistance; Rodwell group members, for advising; my Nanofam, for unmatched friendship and kindness. In particular, I would like to thank my mentor, Cheng-Ying Huang, for providing me with the perfect balance of encouragement and freedom for a successful summer.

References:

[1] Chobpattana, V.; "Nitrogen-passivated dielectric/InGaAs interfaces with sub-nm equivalent oxide thickness and low interface trap densities"; Applied Physics Letters 102, 022907 (2013).