Self-Aligned Germanium TFT Flash Memory

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Abstract/ Introduction:

In recent years, it has become difficult to scale complementary metal oxide semiconductor (CMOS) technology. There are problems with traditional scaling, such as an increase in leakage currents when the devices become smaller. In order to continue to make more efficient and cost effective devices for a growing flash market, new materials are sought, especially to replace the silicon channel. Incorporating a germanium (Ge) channel is an attractive option since Ge has lower effective mass and a higher hole (4X higher) and electron (2X higher) mobility compared with silicon (Si). Using a Ge channel instead of a Si channel done through e-beam evaporation and chemical mechanical polishing to make the surface smoother, a Al_2O_3 tunnel oxide (atomic layer deposition, ALD), Au nanocrystals (e-beam evaporator), Al_2O_3 control oxide (ALD), and Cr gate (e-beam evaporator), this thin film transistor device will be compared with a standard Si thin film transistor in terms of IV and CV characteristics. In addition, the self-aligned design will allow us to use ion implantation without a mask, which saves steps in our design process. Ideally, since Ge performs better in PMOS, it will be used only in PMOS on a CMOS platform.

Experimental Procedure:

First, a mask was used for the alignment marks on the bare silicon wafers. For the resist spinning stage, using P-20 and 1813, we spun at 4000 RPM, 30 seconds; baked at 90°C, 1 minute; used the 5X stepper for exposure; developed using 300 MIF, 90 sec; and postbaked at 115°C 90 sec. Second, we etched the silicon using the Oxford 80-1 using SF_6/ O_2 at 45 sec. Next, oxide deposition via plasma enhanced chemical vapor deposition (PECVD) for 210 nm, followed by germanium deposition from the electron beam evaporator for 100 nm. We also deposited 20 nm Ge layers on some wafers for the control.

For the 100 nm Ge wafers, chemical mechanical polishing (CMP) was done to try to match the 20 nm layer. The CMP recipe that was used was; 4 psi (back pressure), 15 rpm (table speed), 15 rpm (chuck speed), using P-1000 as the slurry, and a poly pad. These wafers showed a low surface roughness rms = 0.122 nm compared with the non-CMP wafers of 0.224 nm from the atomic force microscope (AFM), shown on Figure 1 and Figure 2.

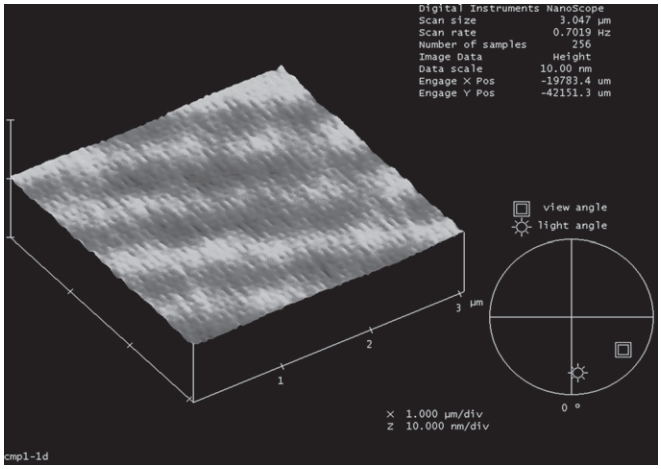

Figure 1, top: AFM. 4psi-15RPM-15RPM; Surface Roughness = 0.122 nm, using Slurry of P-1000 and poly pad.

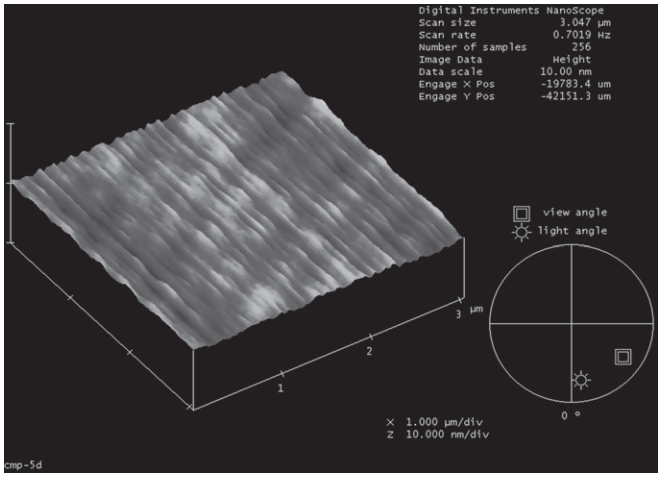

Figure 2, bottom: AFM of non-CMP wafer.

A second mask was used, for the channel area, similar to the process used for the first mask. This was followed by the Ge etch on the Oxford 80-1 using CF_4, LOR spinning and prebake. We used 3000 RPM and tried 45 seconds for spinning, prebaking at 180°C for 5 min. Then exposed with our last mask for the transistor area, which would enable us to do a lift-off resist process, developed with MIF 300 at 90 seconds on some wafers and 120 s on others, and postbaked at 115°C for 90 sec.

Next, several splits were done. For all wafers, we deposited Al_2O_3 using the ALD for the tunnel oxide for 6.3 nm. Next, gold nanocrystals were deposited on some wafers on the e-beam evaporator of 1.2 nm. This was followed by Al_2O_3 deposition for the control oxide of 12.5 nm on some wafers. Other wafers had TiDyO as the control using sputtering.

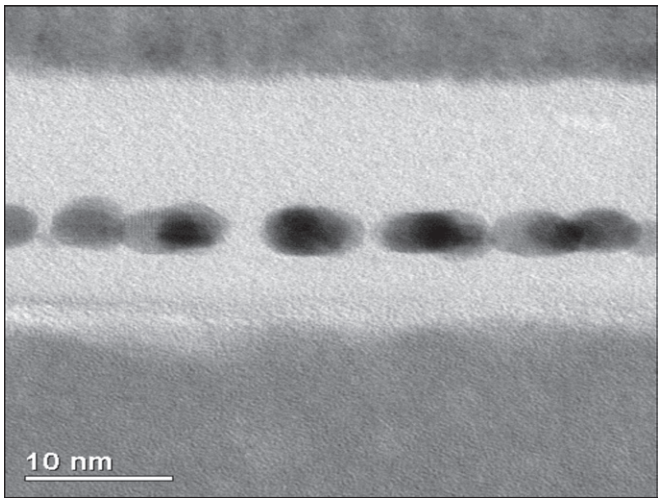

Figure 3: STEM. Bottom to top: germanium channel, Al_2O_3, Au nanocrystals, Al_2O_3, Cr gate.

Lastly, the chromium gate was deposited on the e-beam evaporator for 50 nm. This gate stack can be seen in Fig. 3.

Finally the lift-off process started, dipping the wafers in 1165 for a few hours. In retrospect, the LOR development stage of MIF 300 at 120 seconds was excessive, since it botched the gate deposition. 90 seconds worked better. A picture of this under the scope is seen on Figure 4. Ion implantation was done using the Eaton ion implanter, n-type phosphorous, at 3×10^{15}/sq.cm. Annealing was done to activate the dopants using the rapid thermal annealer for 1 min, 450°C, since the furnace tubes may have oxidized the germanium. Lastly, passivation was performed, using the furnace tunes with H_2/Ar, 400°C for 30 min.

Results/ Conclusion:

A few devices were tested with several different combinations of nanocrystals, and control oxides:

1. Ge(20nm)/Al_2O_3-tunnel/Au/Al_2O_3-control/Cr,
2. Ge(20nm)/Al_2O_3-tunnel/$Al_2O_3$3-control/Cr,
3. Ge(20nm)/Al_2O_3-tunnel/Cr.

The results were not ideal. The I-V curves did indeed look like normal transistor I-V curves except the currents were too low. We skipped the annealing of the germanium due to problems and lack of time. This should be noted for future work.

Future Work:

Annealing was skipped due to the germanium oxidizing. Two theories were given. First, after heating the wafers (right after the germanium deposition), at 600°C 1hr N_2 ambient, the wafers came out of the furnace tubes still hot, and they came in contact with the air, possibly causing oxidation. The second theory was that the oxide layer under the germanium may have been causing it to oxidize. For future work, a nitride layer may be added under and over the germanium layer. Then annealing can be done, since the nitride will cover both sides of the germanium, and the top nitride layer can be removed. Then the normal procedure outlined here can be followed.

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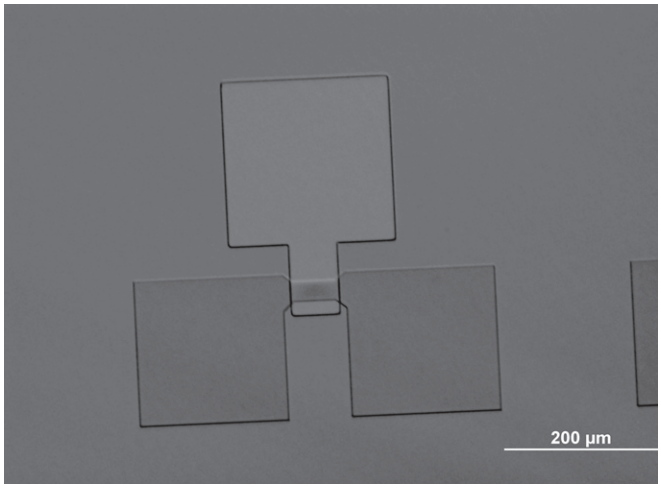

Figure 4: Optical microscope image. Shows the source, drain, gate layout.