Atomic Layer Deposition of Thin Film Hafnium Oxide as Top Gate Oxide in Graphene Field Effect Transistors

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Abstract:

Graphene is a single layer of sp^2-bonded carbon atoms arranged in a honeycomb lattice, which shows some unique electronic properties. Current field effect transistors based on graphene commonly use silicon dioxide/silicon (SiO_2/Si) wafers as a global back gate. In order to locally control the carrier type and density, we plan to fabricate a hafnium oxide top gate. Using e-beam lithography and atomic layer deposition (ALD), we patterned and deposited a 45 nm thick layer of hafnium oxide across single and bi-layer graphene.

Introduction:

As silicon electronics systems get smaller, they will eventually reach a limit as to how small their dimensions can become. There will be a need to find a new material with promising electronic properties on the nanoscale. Currently carbon-based materials display the most promise for these systems. Carbon nanotubes have many of the properties that are sought after in electronics, but controlling chirality and positioning the nanotubes for a circuit is difficult. A newly-discovered form of carbon-graphene, a two-dimensional material, shows great potential for applications in the electronic industry. Graphene, a single sheet of carbon atoms arranged in a honeycomb lattice, possesses a unique linear band structure and has higher carrier mobility than normal silicon devices. One way to make a p-n junction on graphene is to make a top gate oxide.

In previous experiments with a top gate oxide on graphene, a precursor molecule was needed so that Al_2O_3 could be deposited on graphene [1]. The additional molecule layer between graphene and the oxide would change the properties of graphene; this is not ideal for a top gate material. Carriers are produced in graphene by applying an electric field. A positive electric field will cause graphene to be an N type carrier and a negative field will create a P type carrier. This property allows p-n junctions to be made on graphene. The process to make hafnium oxide (HfO_2) top gates uses standard lithography techniques, so current semiconductor manufacturing equipment can be used.

Experimental Procedures:

Thin sheets of graphene were produced by using mechanical exfoliation. A piece of scotch tape was placed on highly ordered pyrolytic graphite (HOPG) and a layer of HOPG was peeled away. The tape was then folded in half and separated several times to spread out and cleave the graphite. The graphite was transferred to a silicon wafer coated with 300 nm of silicon dioxide. The surface of the tape was then rubbed gently with tweezers for 5-10 minutes, after which the tape was removed from the wafer. The wafer was then searched for thin layers of graphene using an optical microscope. Graphene could be optically identified on 300 nm thickness of silicon dioxide because graphene creates interference and contrast with the substrate.

After a suitable sheet of graphene was located, e-beam lithography was used to pattern the features for the top gate on graphene. After development of the e-beam resist, 45 nm of (HfO_2) was deposited using ALD. ALD uses a two precursor gas system that alternates pulses of H_2O and $Hf(NMe_2)_4$. The two gases are pulsed over the graphene surface and when they react they form HfO_2. By changing the number of cycles, we are able to precisely control the thickness. The relatively low temperature of 110°C gave us a smooth film. Since ALD deposits a conformal layer, lift-off was more complicated. Lift-off was accomplished by soaking in warm (40°C) acetone for several hours.

Results and Discussion:

It was found that of the two standard recipes for making hafnium oxide (one 250°C and the other 110°C). They registered approximately 3 nm on the Roughness Measurement System (RMS) and 0.6 nm RMS respectively. The lower temperature recipe, therefore, yields a much smoother film. The roughness of the oxide film is important because it affects the evenness of the electric field and thus the carrier density. Even though graphite is hydrophobic, it was found that it is still possible to grow hafnium oxide on graphite without any coatings.

PHYS

Figure 1 shows an AFM image of a square 4 μm by 4 μm of HfO_2 that was deposited on a few layers of graphene. The hafnium oxide thin film of has a consistent thickness of 45 nm and conforms to the profile of the surface. Figure 2 shows the roughness of hafnium oxide changes depending whether it is on silicon dioxide or graphene. A second sample (Figure 3) was deposited under the same conditions, but lift-off consisted of only warm acetone. This yielded a cleaner SiO_2 surface in addition to lifting off the HfO_2. The HfO_2 is still rougher on graphene then on SiO_2. Figure 3 is an AFM image of the second trial. Figure 4 shows that the hafnium surface is still a little rougher on the graphene.

Future Work:

Primarily, we hope to improve lift off conditions. We hope to achieve this by decreasing the thickness and increasing the undercut. Moreover increasing the soaking temperature and possibly experimenting with sonication time could also help. Once lift off conditions are reliable the next step would be to test the effectiveness of the top gate oxide for carrier injection.

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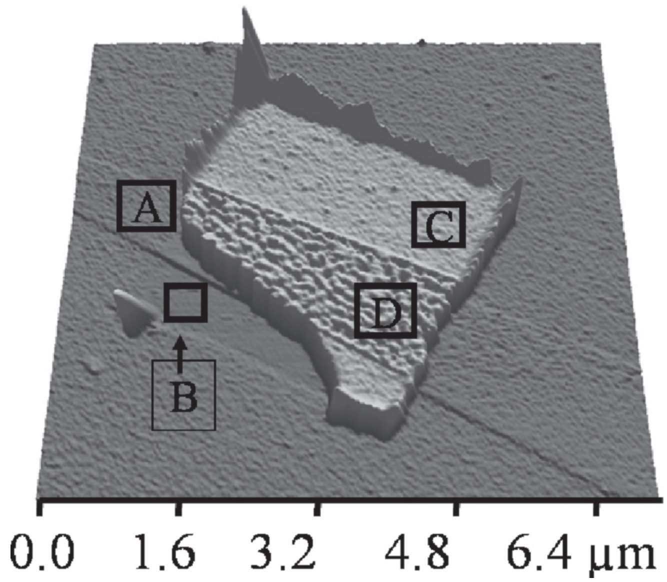
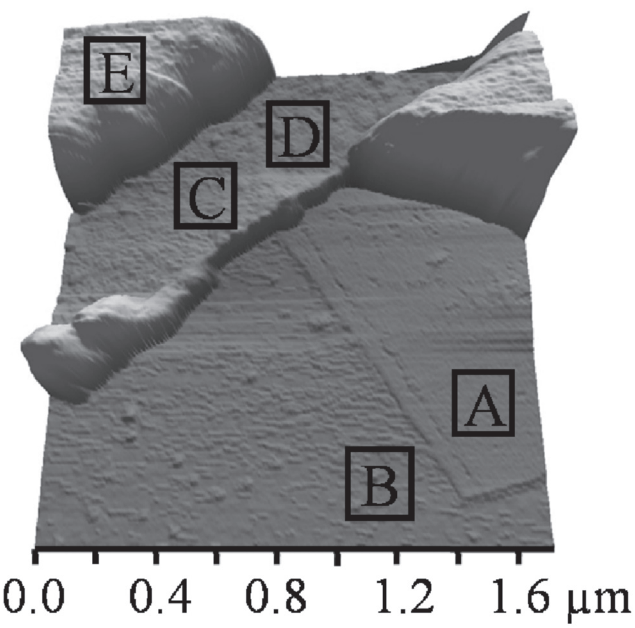


Roughness RMS [nm]		Surface Type
A	0.4	Few layers of graphene on SiO_2
B	0.6	SiO_2 surface that was underneath HfO_2
C	1	45 nm of HfO_2 on top of SiO_2
D	3	45 nm of HfO_2 on top of few layers of graphene



Roughness RMS (nm)		Surface type
A	0.5	Few layers of graphene on SiO_2
B	0.8	SiO_2 surface that was underneath HfO_2
C	1	50 nm of HfO_2 on top of SiO_2
D	1.2	50 nm of HfO_2 on top of few layers of graphene
E	---	HfO_2 on resist

TOP
Figure 1: AFM image of HfO_2 on graphene.

Figure 2: RMS values for Figure 1.

BOTTOM
Figure 3: AFM image of the second deposition of HfO_2 on graphene.

Figure 4: RMS values for Figure 3.