Development and Optimization of Pulse Plating of Copper Films for MEMS Applications

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Abstract:

High-aspect-ratio copper structures are important in the fabrication of heat dissipaters, heat sinks and radio frequency (RF) antennas among many other microelectromechanical systems (MEMS) devices. Electroplating is a preferred technique for coating thick films (> 1 μm) on metallic surfaces. The properties of the plated films are improved by the use of pulse plating. In pulse plating, the potential or current is alternated between two different values. The goal of this project is to develop and optimize a process for pulse plating copper on a patterned wafer. The challenge is to plate high aspect ratio, high quality features that are commonly required in the MEMS processes. Forward-reverse cycling enhances film characteristics such as roughness, low stress, uniformity and conformality. The optimum conditions for pulse plating a patterned wafer were determined.

Introduction:

The deposition of a metallic coating onto an object is achieved by putting a negative charge on the object (cathode) to be coated and immersing it into a solution (electrolyte) which contains a salt of the metal to be deposited. The metallic ions of the salt carry a positive charge (cations) and are thus attracted to the cathode which provides electrons to reduce the positively charged ions into a metal atom.

Copper plating is the critical step in through-wafer interconnects, which is becoming a promising new alternative for a wide variety of applications such as 3D integrated circuits, MEMS packaging and high frequency applications [1]. Filling of high aspect ratio vias has to be mastered before the technology is available. Bottom-up copper plating into the vias is the critical step to fill through-wafer vias. Other MEMS applications such as heat sinks and RF antennas also require high quality copper films. In the last case the requirements are more stringent, in addition to void free, low stress and highly conformal films the side walls must be very smooth. This can only be achieved by the use of pulse plating [2].

The objective of this work is to develop and optimize a pulse-plating process to be used in this facility.

Experimental Procedure:

The plating process included: surface preparation, electro-plating, photoresist removal and analysis.

Surface Preparation. Standard 4" silicon (Si) wafers were seeded with 3000Å of copper by sputtering it over 300-500Å of Cr in a EnerJet sputter-coater. The back of the wafers had been, previously, electrically isolated by depositing a plasma enhanced chemical vapor deposition (PECVD) film of Si-oxide. The wafers were patterned using 10000Å film of AZ 9260 photoresist. The samples were exposed in a Suss MA6 aligner. After exposure and development the wafers were inspected using an optical microscope and the areas to be plated carefully measured.

Electrochemistry. The Pyrex® electrochemical cell, Teflon® lid and electrode holders were leached with diluted sulfuric acid to remove all contaminating ions. The anode material, a (0.027") copper plate 4 × 4" 99.9% pure, prior to use, was degreased with IPA and then etched with ammonium persulfate and soaked in 10% volume sulfuric acid to remove surface oxide, and finally, rinsed with de-ionized (DI) water. The electrolyte was a commercially available plating solution from Enthone Corp., MICROFAB® SC Make-Up and a brightner, MICROFAB SC MD. The cell was kept at 24°C while agitated at 200 rpm. The electrical contact, to the front of the wafer, was done by means of a stainless steel tweezers cut and bent to provide a tight contact. Care was taken to make sure that the electrolyte did not touch the electrical contact.

The DC programmable-pulse power supply used was a Dynatronix® DuPR MicroStar. The in-put variables were: I_{fwd}, actual (cathodic) plating current (13 to 43 mA/cm^2); I_{rev}, reverse (anodic) or stripping current (-20 to -63 mA/cm^2); t_{fwd} was the actual plating, ON, time; and t_{rev} was the time OFF or the negative pulse duration. The plating was done at constant current. After plating was completed, the samples were removed from the plating bath, and rinsed thoroughly with DI to avoid the appearance of stains on the surface.

Post Plating. Removal of the photoresist was done using PRS 2000. Samples were soaked for 5 min, then thoroughly rinsed and dried. The roughness and thickness were measured in an

HRP-200 KLA-Tencor profilometer. Some samples were also put in a SEM (FEI-Quanta) in order to examine the walls, corners and grain size of the plated features.

Results:

In Figure 2 and 3, the conditions were: i_{fwd} = 13 mA/cm^2; t_{fwd} = 15 ms; i_{fwd} = -27 mA/cm^2; t_{rev} = 1 ms, plating time 20 min.

In Figure 4, the conditions were: i_{fwd} = 17.76 mA/cm^2; t_{fwd} = 15 ms; i_{rev} = -26.64 mA/cm^2; t_{rev} = 1 ms, plating time 25 min.

Conclusion and Future Work:

A process for pulse-plating copper onto a patterned Si wafer was developed. The process deposition rate is 4000Å/min. The films obtained are uniform, void free and highly conformal. The roughness of the deposited films needs further study. It has been reported in the literature [3] that the roughness of the surface is also due to the seed layer oxidation. This oxide should be removed prior to electroplating to ensure uniformity. The dependence of the brightner and roughness should also be studied.

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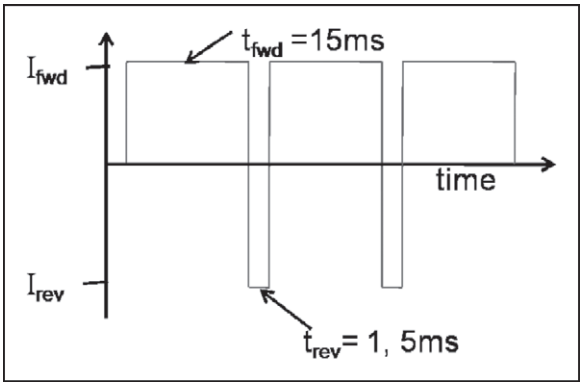

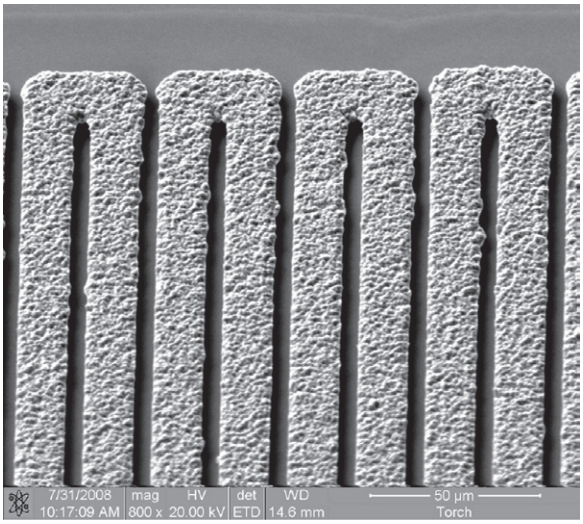

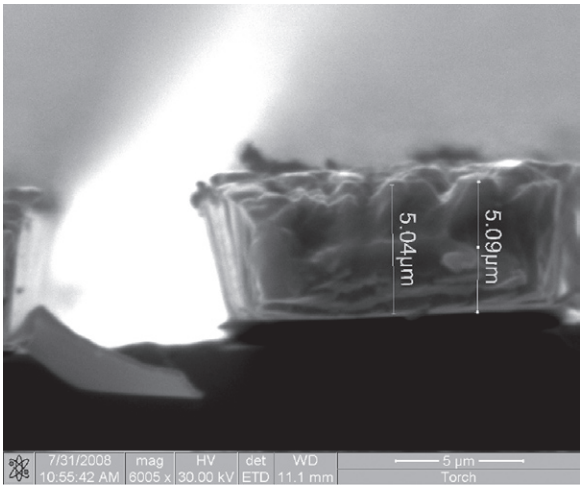

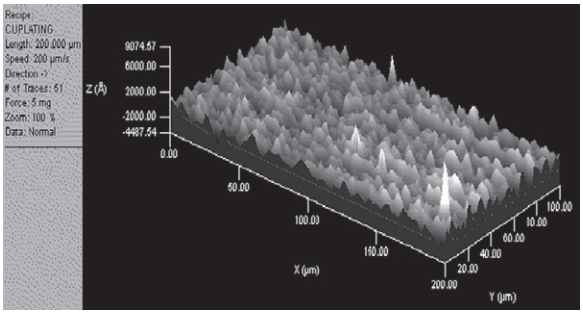

Figure 1, top: Pulse cycle.

Figure 2, upper middle: SEM photo showing conformality.

Figure 3, lower middle: SEM photo showing void free walls.

Figure 4, bottom: Profilometer photo of roughness of the deposited films.