# Heterogeneous Integration of p- and n-type Nanowires for Complementary Nanowire Circuits

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## Abstract:

**Nanowires have shown promising results for use in creating future electronic devices that go beyond the end of metal-oxide semiconductor field effect transistor (MOSFET) scaling and for the use in three dimensional (3D) complementary circuits. Our efforts here focused on the optimization of the nanowire contact printing method, a critical step for fabricating nanowire field-effect transistors (NW FETs) at large scale. NW FETs have been studied extensively by Professor Lu's research group at the University of Michigan [1]. The parameters of the contact printing optimized here were the applied pressure of the nanowires on the substrate, the lubricant applied to the nanowires, the distance traveled by the substrates and the average speed of the transfer process. We also demonstrated and studied simple NW FETs based on these optimization efforts, which showed comparable performance to previously constructed devices. Using this optimized method, a simple integration process could be used to combine two types of NW FETs, one SnO2 n-type and the other Ge/Si core/shell p-type, for possible 3D complementary nanowire circuit applications. 3D circuits can offer a larger integration density, faster operation speed and lower overall power consumption than current MOSFET technologies [2].**

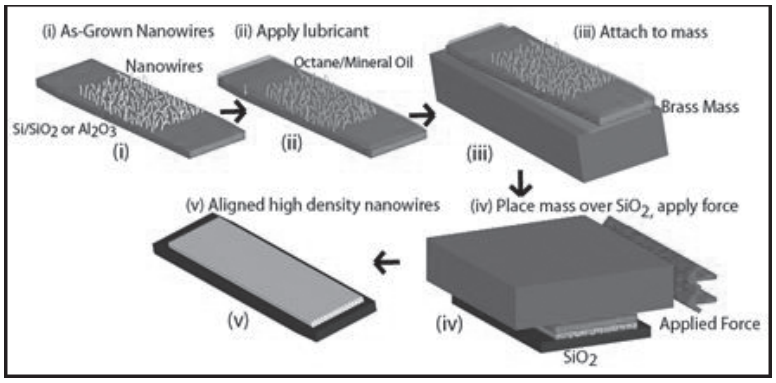


*Figure 1: Diagram of contact transfer method.*

## Experimental Procedure:

The nanowire contact printing transfer method works by using two competing forces, the van der Waal's force of attraction and the application of an external mechanical shear force to cause the nanowires to be deposited on a device substrate. The details of the contact transfer process are described in Figure 1.

We began the transfer process by taking a growth substrate of as-grown nanowires and applying a layer of lubricant with a specific ratio of octane and mineral oil. Secondly, a brass mass, whose total mass was determined by the desired applied downward pressure, was attached to the growth substrate. Thirdly the mass, with the growth substrate firmly attached was placed in direct contact with the device substrate, which caused the nanowires to loosely adhere to the device substrate by the van der Waal's forces of attraction. Thirdly, a micrometer applied an external shear force onto the brass mass, which caused the growth substrate to slide over the device substrate. The opposing competition of the van der Waal's force and applied shear force resulted in the breakage of the nanowires at about midway of the nanowires' total length.

The broken nanowires were then aligned on the device substrate in the direction of the external shear force. The lubricant layer was then gently rinsed off with acetone and isoproponal, and left to air dry.

The resulting nanowire layer was then ready to be used in the fabrication of a nanowire transistor. In order to quickly analyze and characterize the Ge/Si core/shell nanowires, a simple back gated transistor was fabricated using standard photolithography procedures and nickel contact deposition. Nickel was chosen as the contact for these nanowires so that the p-type Ge/Si core/shell nanowire created an ohmic metal-semiconductor interface. The $SnO_2$ device was fabricated using a top gate approach with gold contact deposition in order to simulate the actual device used for fabricating a 3D complementary circuit.

| Parameter | Low Effect | High Effect | Explanation |
|---|---|---|---|
| Distance upon which shear force is applied | Low surface area of transferred nanowires with overall high density | Larger surface area of transferred nanowires but transferred density decreases with increasing distance | Nanowires are initially transferred during the beginning of the sliding process, leaving less nanowires on the growth substrate to at farther distances |
| Applied Downward Pressure | Longer, less aligned nanowires with a lower nanowire transfer density | Shorter, more aligned nanowires with a higher overall nanowire density | Increased pressure causes stronger nanowire adhesion to the receiving substrate which causing the nanowires to break more easily |
| Composition of Lubricant | Less viscous lubricant causes a higher transfer density with shorter, less aligned nanowires | More viscous lubricant causes a lower transfer density with longer, more aligned nanowires | More viscous lubricant causes the nanowires to be suspended within the lubricant layer and not strongly adhered to the $SiO_2$ causing the lower transfer density and the longer, aligned nanowires |
| Lubricant Removal | Less of a rinse in acetone and isoproponal does not remove the applied lubricant layer | Higher amounts of rinsing in acetone and isoproponal causes the transferred nanowires to become unaligned and less dense | Increased forces applied by the higher quantities of the lubricant removal causes the nanowires to detach from the $SiO_2$ substrate while the lower quantities do not remove the lubricant fully |

*Table 1: Observations of modified contact transfer parameters.*

| Nanowire Diameter | Applied Pressure | Applied Lubricant | Distance Moved | Speed Traveled |
|---|---|---|---|---|
| 20 nm | 5 psi ($SnO_2$) 10 psi (Ge/Si) | 1 drop of 2:1 v:v octane/ mineral oil | 3 mm | .5 mm / min |

*Table 2: Optimal nanowire transfer parameters.*

## Results and Discussions:

The observations of the distance, force, lubricant composition and lubricant removal are shown in Table 1 with the optimal nanowire transfer conditions shown in Table 2. These conditions provided high density aligned nanowires that were of good length for fabricating NW FETs. An SEM image that displays the good alignment, density and length of the optimized $SnO_2$ transferred nanowires is shown in Figure 2 (i).

The nanowire field effect transistors fabricated from the optimal transferred nanowires showed comparable performance to recently fabricated nanowire transistor devices [1]. The back-gated Ge/Si core/shell device carried a fair amount of current and displayed a gate response even though the gate dielectric was thick at 600 nm. The device did not display linear IV behavior as was expected, which could have been due to Schottky effects at the Ni-nanowire contacts as seen in Figure 2 (iv). The top-gated $SnO_2$ device demonstrated a strong gate response, as expected, but appeared to not reach saturation as the device current continually increased with the source-drain voltage which is seen in Figure 2 (iii).

## Future Work:

In order to combine the n-type $SnO_2$ nanowire field-effect transistor and the p-type Ge/Si nanowire field-effect transistor, we first must be able to get increased performance from the devices separately. This can be accomplished by optimizing the fabrication process and ensuring that the properties of the as-grown nanowires are unaffected by the transfer process. After finishing fabricating the separate NW FETs, the two can be combined by placing a separate $SiO_2$ isolation layer over the $SnO_2$ device, and fabricating the Ge/Si device on the $SiO_2$ isolation layer. After this process is completed, we can test to see if the $SnO_2$ device performance or geometry is affected by the isolation layer or the fabrication of the second layer Ge/Si device.

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## References:

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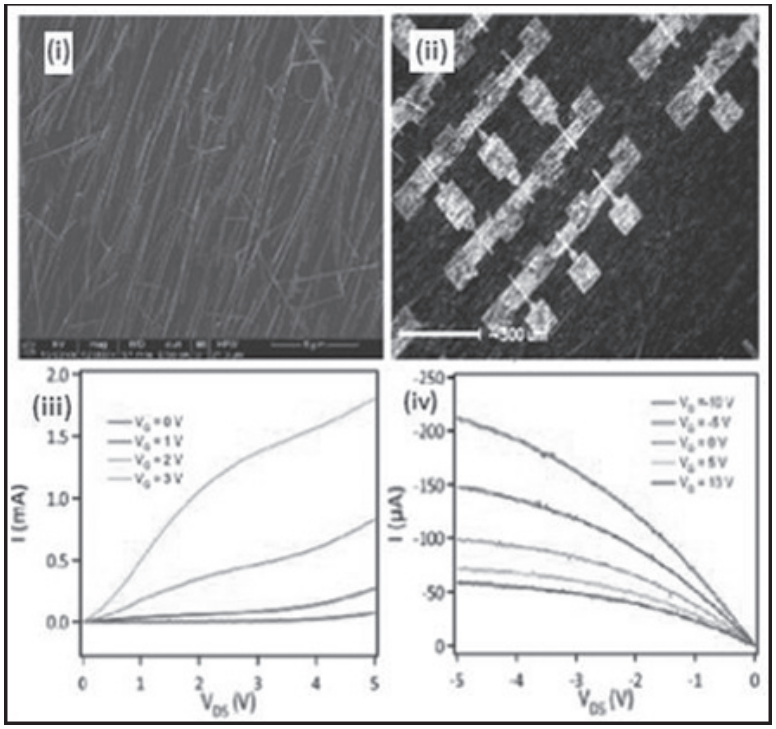


*Figure 2: (i) Optimal transferred $SnO_2$, (ii) $SnO_2$ device nanowires, (iii) IV curve of n-type device, and (iv) IV curve of p-type device.*