

Thermally Enhanced Dynamic Core Migration with Phase Change Materials

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Abstract:

Due to the presence of hotspots in microprocessors, localized cooling solutions have become a significant area of research. This study's aim was to fabricate a chip containing heaters of varying size, to simulate these hotspots. Resistance temperature devices (RTDs) were fabricated around these heaters to measure the temperature of the hotspots and the heat spread through the substrate. The chip will be used to characterize the ability of various phase change materials (PCMs) to mitigate the effect of transient hotspots. Fabrication included electron beam deposition, plasma enhanced chemical vapor deposition (PECVD), and reactive ion etching (RIE). Material deposition consisted of titanium (Ti), as a layer of adhesion, and platinum (Pt), as the sensing material. The devices were calibrated to determine the relationship between temperature and the electrical resistivity of the heaters and RTDs.

Introduction:

Hotspots are areas of high heat flux and high temperature. Certain areas of a chip consume more power by performing more processes, and therefore these hotspots form [1]. After reaching the threshold temperatures, the chips must be allowed to cool to avoid damage from the hotspots. A localized cooling solution would lengthen the amount of time the device could be used, and make the device more efficient.

A chip containing eight heaters of varying size was fabricated to imitate these areas. Surrounding these heaters are several RTDs to measure the heat spread through the substrate of the chip.

Method:

A layer of negative resist, NR9-1500PY, was spun on a Pyrex® wafer in order to deposit metal in the pattern of the mask on the wafer. Pyrex wafers were employed as the substrate due to the fact that they have a low thermal conductivity, and therefore minimize heat spread. The resist was exposed and developed. Then Ti and Pt were deposited using e-beam deposition. Ti was deposited as an adhesion layer, and Pt as the sensing material. Pt is an extremely accurate material for use in RTDs. The resist was then removed, leaving only the first layer of the devices. Next, a layer of negative resist, NR9-8000, was spun on the wafer. It was then exposed and developed. Ti was again deposited for adhesion purposes, followed by copper (Cu) and then gold (Au), using e-beam deposition. Cu was utilized as a high conductivity material for the leads of the device, and Au was needed in order to wire bond the device for testing. The resist was removed, leaving the final layer of the devices.

To characterize this device, the resistance of the RTDs and the heaters must be measured and compared to one another. In addition, the electrical resistivity of the devices versus temperature must be calibrated.

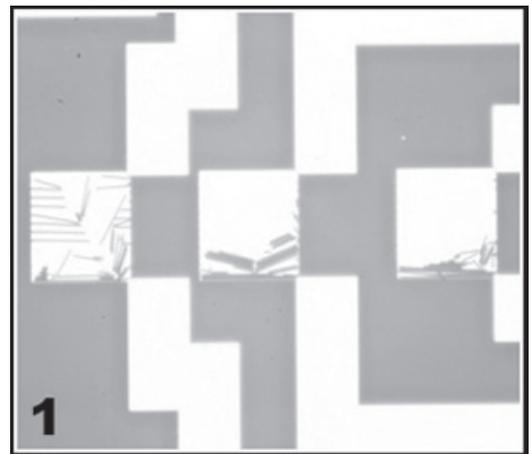
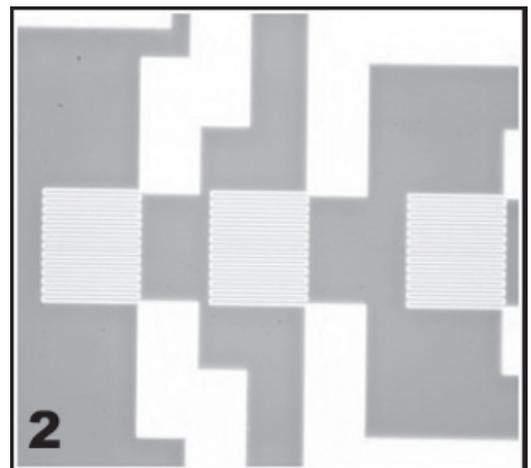


Figure 1, above: Devices are damaged due to improper adhesion. Figure 2, below: Devices are intact due to proper adhesion.



Results and Discussion:

One major fabrication difficulty was obtaining correct resist adhesion to the wafer. Normally, the resist used is heated on a hotplate. However, since Pyrex has a low conductivity, a temperature gradient would be produced between the bottom and the top of the wafer. To avoid this, the wafer was soft baked in an oven to achieve uniform heating. The bake time was recalculated to account for this alternate form of heating.

It was seen that many of the devices appear damaged after development, as seen in Figure 1. These devices were found consistently in the center of the wafer. At first, the wafer was placed on a dish in the oven to bake. The dish caused the devices to heat unevenly in the center of the wafer, causing the resist to bake improperly, and thus detach from the substrate. Instead, the wafer was placed on several dishes so only the edges of the wafer, where no devices were present, would be in contact with the dishes. This method produced fully developed devices over the entire wafer, as shown in Figure 2.

An oxide layer was deposited to protect the leads of the device. A small area of the leads was etched using RIE to expose the metal for testing. However, it appeared the etching was extremely uneven. Certain leads appeared to have oxide present, while other areas showed signs of metal being etched. Therefore, it was decided to test future devices before the oxide layer was deposited.

After calibrating the resistance of the devices versus temperature, it could be seen that the resistance of the heater wires was much lower than the average resistance of the RTD's, as seen in Figure 3. This was due to the fact that the cross-sectional area of the heater was much greater than that of the RTD.

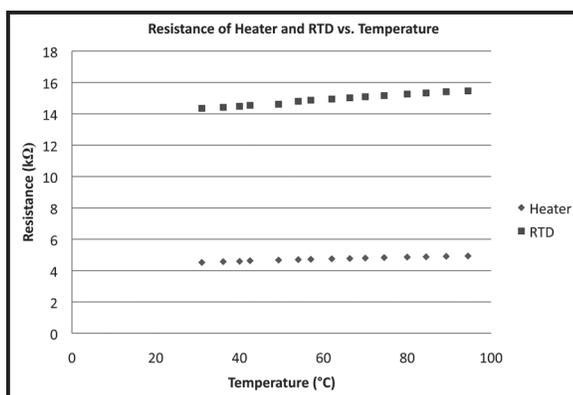


Figure 3: Resistance of heater wires is much lower than the resistance of the RTDs.

The relationship between resistance and area can be seen in Equation 1, where R is resistance, ρ is resistivity, l is length, and A is the cross-sectional area:

$$R = \rho \frac{l}{A} \quad (1)$$

Conclusion:

The oxide etch process needs to be researched further in order to provide uniform etching over the wafer. Continued testing of this heater device will allow possible cooling solutions to be tested utilizing an accurate hotspot simulation.

Future Work:

One cooling solution that is being researched currently is the use of phase change materials (PCMs). A phase change material is a material with a melting temperature at or around the working temperature of the device that it will be implemented in. Thus, when the device reaches its working temperature, the PCM will melt, absorbing thermal energy and cooling the device. A chip utilizing PCMs will be fabricated and tested, using the heaters as hotspot simulations.

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References:

- [1] Link, G., Vijaykrishnan, N.; "Hotspot Prevention Through Runtime Reconfiguration in Network-On-Chip" (2005)