Fabrication and Characterization of Indium Arsenide Nanowire Transistors

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Abstract and Introduction:

III-V compound semiconductors such as indium arsenide (InAs) have long been known to have favorable electronic properties such as high electron mobilities. For this project, top-gated transistors were fabricated from InAs nanowires using a lanthanum lutetium oxide ($LaLuO_3$) high-κ dielectric in a horizontal geometry. The InAs nanowires were all grown by molecular beam epitaxy (MBE), and some nanowires were n-doped with silicon, using beam flux values corresponding to doping calibration of layers.

These transistors were then characterized by I-V measurements using a DC probe station. The gate influence was clearly visible in these I-V measurements, and cutoff was observed at sufficiently negative biases. Additionally, attempts were made to perform C-V measurements. However, these attempts proved unsuccessful due to parasitic contributions from the contact pads and the substrate.

Experimental Procedure:

First, a silicon (Si) substrate with an oxide layer was pre-patterned with alignment marks using photolithography. Previously-grown nanowires with different intentional dopings were then transferred onto predefined regions of the substrate such that each region contained wires of a known single doping. The wires were transferred by physically contacting them with cleanroom paper and then contacting a region of the target substrate. Because this leaves the nanowires in a random arrangement, a scanning electron microscope (SEM) was used to locate suitable nanowires on the substrate in relation to the alignment marks.

From there, electron beam lithography with a poly(methyl methacrylate) (PMMA) resist was used to pattern source/drain contacts on the nanowires. A brief argon sputtering was used to etch away the native oxide from the nanowires, and the gold (Au) contacts were then deposited with a titanium (Ti) adhesion layer. 50 nm of $LaLuO_3$, a high-κ gate dielectric, was then deposited over the entire sample using pulsed laser deposition. Ti-Au gate contacts were then patterned using e-beam lithography and metal deposition. An SEM of a typical device is shown in Figure 1.

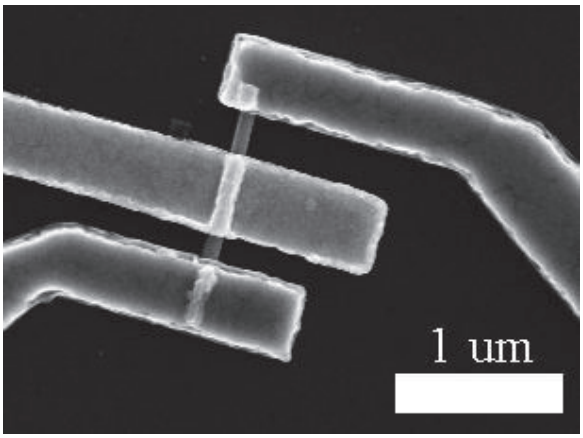

Figure 1: SEM of a typical top-gated InAs nanowire transistor.

Various I-V measurements were then performed on all of these devices using a DC probe station. Attempts were also made to perform C-V measurements on the gates using an impedance analyzer.

Results and Conclusions:

Direct current (DC) measurements showed that approximately 60% of the devices fabricated were non-functional. However, for all the devices that were functional, the gate influence was clearly visible, with higher drain currents at higher gate voltages for any given source-drain voltage, a behavior indicative of n-channel devices. The drain current response of a typical device during a gate voltage sweep is shown in Figure 2. The drain current response of another typical device during a source-drain voltage sweep is shown in Figure 3. All devices showed a threshold voltage of approximately -4V, as illustrated in Figure 3.

The nanowires' resistances were measured to be generally between 15 kΩ and 1500 kΩ for both undoped and n-doped nanowires. Given an average nanowire diameter of approximately 100 nm and device lengths of about 1000 nm, we can calculate the resistivity of the wires to be between approximately 0.01 Ω cm and 1 Ω cm.

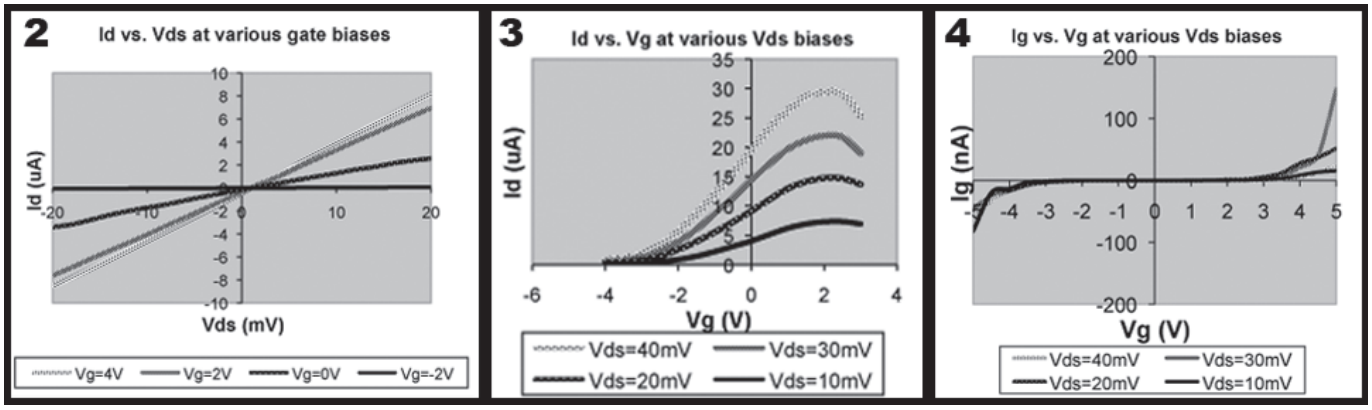

Figure 2: I_d-V_{ds} response of a top-gated nanowire transistor at various gate biases. The nanowire was undoped.

Figure 3: I_d-V_g response of a top-gated nanowire transistor at various source-drain biases. The drop in I_d at higher gate voltages is likely a result of the gate voltage being swept from high to low in this instance. The nanowire was undoped.

Figure 4: Gate leakage current as a function of V_g at various source-drain biases. The nanowire was n-doped with a Si beam flux corresponding to 1×10^{17} cm^{-3} in layers.

The peak gate transconductance was computed at several source-drain biases. At a 40 mV source-drain bias, the peak gate transconductance was about 4 μA/V, accurate to within a factor of two. However, the accuracy of the doping process has not yet been experimentally confirmed, and the contact resistance has not yet been de-embedded. Thus, no mobility values can yet be confidently reported.

We also measured the gate leakage current, which varied substantially from one device to another. In most cases the leakage current would remain under 100 nA for gate biases between -4V and +4V, as illustrated in Figure 4, however the variation between individual devices was quite substantial.

Attempts to measure the C-V response of the devices' gates were unsuccessful; even with an open compensation parasitics from the contact pads and the substrate were overwhelming. While the expected capacitance response was on the order of femtofarads or attofarads based on previously reported values [1], the parasitic capacitance was on the order of picofarads. Moreover, the parasitic capacitance was not constant due to depletion of the underlying silicon substrate, further complicating any possibility of de-embedding.

Future Work:

Further investigation is necessary to extract parameters such as mobilities. However, the exact doping levels of the nanowires in relation to the dopant beam flux remains an open question. This will be resolved by analysis of both this data and forthcoming measurements. The contact resistance must also be de-embedded. From there, further studies may be done to see how relevant factors, such as a nanowire's doping, length and width, affect device performance.

Additionally, high-frequency measurements would provide valuable insight about such devices' suitability for high-performance electronics. As for C-V measurements, an alternate setup such as a capacitance bridge may overcome the parasitics. Another option is to rebuild these devices on a completely insulating substrate.

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References:

[1] Alexandra Ford et.al., "Diameter-Dependent Electron Mobility of InAs Nanowires", Nano Letters 2009, 9 (1), 360-365.