Fabrication of a Gallium Nitride Nano-Field Effect Transistor

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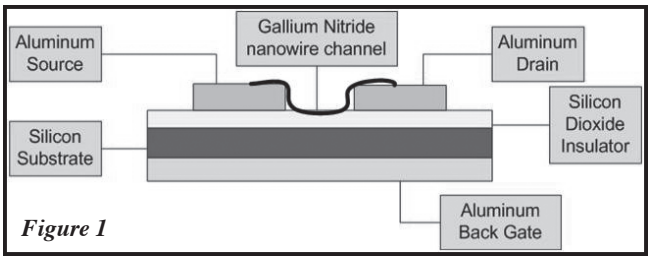

Figure 1

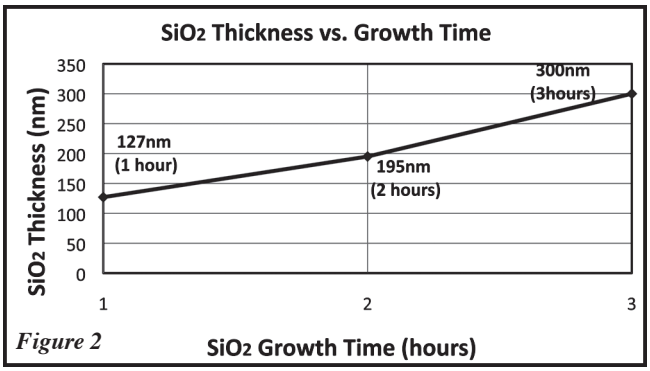

Figure 2

Abstract and Introduction:

The complimentary metal oxide field effect transistor (CMOSFET) continues to be an impacting device within the semiconductor industry. Known for its amplification and switch like capabilities, the MOSFET has great significance in logic circuits, which is central to the operation of computing systems. Components forming the MOSFET include a source, drain, channel, and gate (Figure 1). Miniaturizing such technology to the "nanolevel" has been of great interest to the semiconductor industry. Since the beginning of the twenty-first century, and even before, there has been a push in the semiconductor industry towards the miniaturization of devices. This miniaturization would lead to the compacting of more devices on a single chip, decreased chip size, increased speed and decrease overall component and finished product size. However using the prediction of Moore's law with the present technology, by the year 2020, the steadfast approach to miniaturization will reach its limitations.

Nanotechnology, which some view as the new era in technology, presents us with the possibility to surmount this barrier. Hence, the focus of this research was to demonstrate the use of gallium nitride (GaN) nanowires to fabricate a CMOSFET using the nanowire as the conducting channel.

Methodology:

Fabrication of the nanoFET was initiated with a low resistant, highly doped silicon (Si) wafer, which was cut into one inch^2 pieces. These Si wafers were then thermally oxidized in a quartz furnace at 1100°C to form a layer of silicon dioxide (SiO_2), which will be used as the gate dielectric. The thickness of the grown SiO_2 layer was measured by ellipsometry. For this project, SiO_2 layers of thickness between 275-300 nm were used (Figure 2).

To form the gate contact, a 150 nm thick aluminum (Al) ohmic contact layer was deposited onto the backside of the Si wafer by electron beam evaporation. Prior to evaporation the backside of the wafer was cleaned with hydrogen peroxide to remove any extraneous oxide from the surface. To protect the layer during subsequent fabrication processes, a layer of photoresist was spun onto the surface and baked for 30 mins. Employing photolithography, the source and drain electrodes for the nanoFET were defined atop the SiO_2 layer. We then evaporated 150 nm of Al, or gold (Au), over this surface. A liftoff process was then used to form the source drain contacts. The mask used in this work was specifically designed to maximize the probability of getting nanowires across the source and drain.

The GaN nanowires used were grown in house and measured roughly 50 nm in diameter and 10-100 μm in length. The GaN nanowires were suspended in toluene to aid in their dispersion across the wafer when applied. Using a syringe, the solution was dropped onto the wafer surface where many source-drain contacts were. The solvent was allowed to evaporate, and the sample was then examined under an optical microscope and a scanning electron microscope to confirm nanowire placement on the source-drain contacts (Figure 3).

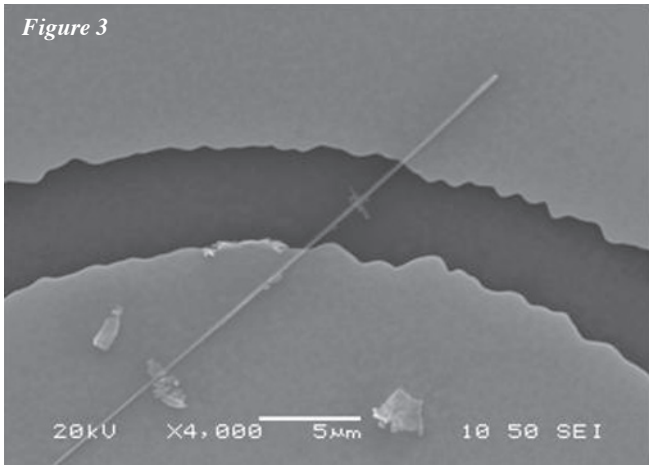

Figure 3

Results:

With many source-drain contacts on each wafer, only a few nanowires landed across the source and drain. Of those which did, electrical contact was not made when tested with an I-V curve tracer. After applying a large voltage across the contacts, some devices began to conduct current, which served to burn-in the metal-nanowire interface, which may have been contaminated by metal and/or nanowire oxides or toluene residue. This is the main reason why Au was substituted for Al.

Figure 4 is the I-V curve of a working device. Application of low voltages is typically indicative of a nanowire channel. The graph resembles a back to back diode, and is applicable for this device.

Along with applying voltage to the source and drain, a voltage was also applied to the backgate to modulate the channel current. However after a number of attempts with different nanoFETs, modulation was not achieved. This was most likely due to the nanowire floating above the oxide surface instead of resting on the oxide, and the thickness of the oxide.

Conclusion:

Oxidation rates for SiO_2 were determined and gate oxides were successfully grown. I-V measurements confirmed the existence of a source-drain channel in the nanowire. Although we were unable to modulate the nanowire channel in our devices, we were able to fabricate GaN nanoFETs using conventional fabrication processes. Although the method of depositing nanowires by dropping them in solution needs improving, nanowire were deposited this way. Perhaps a different solvent would help. To insure nanowires-oxide contact in the future, the source and drain spacing could be widened to allow the nanowires to hang down and the thickness of the source-drain contacts could be made thinner.

Acknowledgements:

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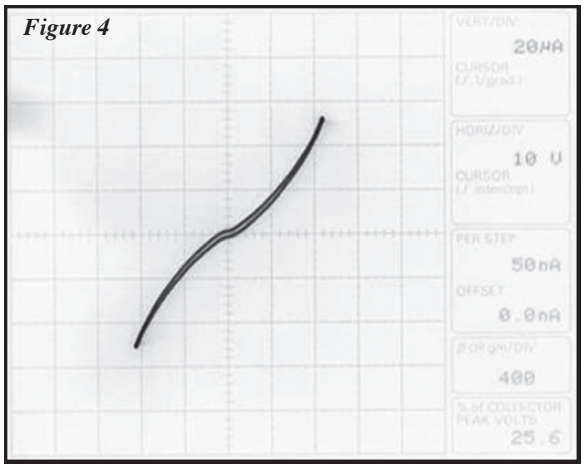

Figure 4