Manufacture of Nanoscale Imprinting Stamps using Electron Beam Lithography

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Abstract:

This project has focused on characterizing all of the processes leading from a bare silicon wafer to the ultimate use of stamps to pattern interconnects for electronics on the 20-100 nm scales. We created our initial patterns in hydrogen silsesquioxane (HSQ) using e-beam lithography. We then used reactive ion etching (RIE) to transfer the patterns onto a silicon wafer. This wafer was coated in a fluorinated anti-stick layer and then used as a stamp to transfer interconnect-patterns into PMMA.

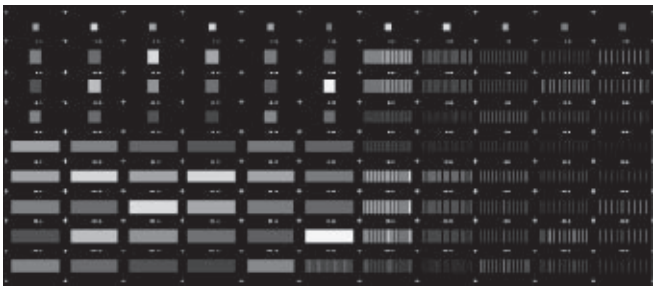

Figure 1: 1000 nm lines with 1:1 pitch are bottom left, single pass lines with 50 µm pitch are top right.

Introduction:

Electron beam lithography (EBL) is a key process that has been used to fabricate nanoscale patterns on a variety of substrates. Though e-beam lithography is a very powerful tool in the laboratory, the process is far too slow to be used in industry.

Nanoimprinting lithography is a method that has recently been investigated to bring the small scale patterning capabilities of e-beam lithography to speeds acceptable for mass-manufacture.

Miniaturization has been the key force driving the constant increase in computing power that we have enjoyed over the past sixty years. As we continue to reduce the scale of our computing devices, we are forced to develop new techniques and strategies. Photolithography reaches its theoretical limit at ~ 32 nm using current proposed methods.

Experimental Procedure:

The fabrication process was broken up into three main steps; each step would undergo a series of optimizations so that the result could be used to optimize the next step in the process.

We started our process by spinning a layer of HSQ, a negative e-beam resist, onto the surface of a 4 inch silicon wafer. At this stage of the process there were a number of parameters we experimented with to produce better results. We used an e-beam pattern with line gratings of differing line thickness and pitch (Figure 1) and a scanning electron microscope (SEM) to optimize our doses for minimal backscattering. During this step we also tried different resist thicknesses and development conditions.

The next step in our process focused on plasma processing. The goals of this step were to reduce the linewidth further by using an isotropic CF_4 chemistry, and then to successfully transfer the pattern from the resist into the silicon substrate using an anisotropic O_2 plasma chemistry. By varying the plasma chemistry and then observing the results under SEM, we were able to adapt existing chemistries to our need. By reducing the DC bias and increasing the chamber pressure, we produced a more isotropic CF_4 etch. We also determined the etch rates of each plasma chemistry and used this data to vary stamp thickness in our next step.

We also experimented with an SF_6 linewidth reduction etch, but the silicon was being etched with the resist and the results were poor. We decided to focus on the CF_4 etch due to time concerns.

The next phase of our procedure was the nanoimprinting step. Features on this scale could only be imprinted if they had been successfully fabricated in an earlier processing step. In this step we used an Obducat nanoimprinter. To prepare our stamp for imprinting, we spun on a thin layer of a fluorinated anti-stick. To prepare our stamping substrate, we spun an oxide wafer with a polymethyl

methacrylate (PMMA) film. We used the oxide as an adhesion layer between the silicon and the PMMA. We varied the thicknesses of the various layers, as well as imprinting temperature, pressure, and time. We observed the results under SEM.

Results and Conclusions:

Using e-beam lithography we managed to achieve sub 10 nm lines with some consistency; below 10 nm, lab conditions prevented accurate imaging. We determined that a higher concentration developer for a longer development time provided a sharper contrast curve.

Using a CF_4 plasma chemistry, we were able to reduce the line thickness from 11 nm to 7.8 nm. The CF_4 linewidth reduction quantity was shown to be a linear function of time, which would allow the overall thinning to be controlled.

Using a silicon etch we were able to confirm the presence of 30 nm features in silicon for use as imprinting stamps. We found that our silicon etch had an etch rate of 29 Å/second and a selectivity of silicon to HSQ of 8.6 to 1.

The nanoimprinting step presented the most difficulty; especially because it could only be attempted after the previous steps had been refined. We were able to imprint 81 nm lines with 500 nm pitch.

Future Work:

Future work would consist of further optimization of each step. Nanoimprinting would then be used to fabricate sub 32 nm interconnect by producing an imprinted pattern with an e-beam dosage and development conditions calculated using our first step of optimization, a plasma chemistry refined in our second step, and an imprinting process used in our last step. The resulting negative would then go through a lift-off process to produce a testable interconnect pattern.

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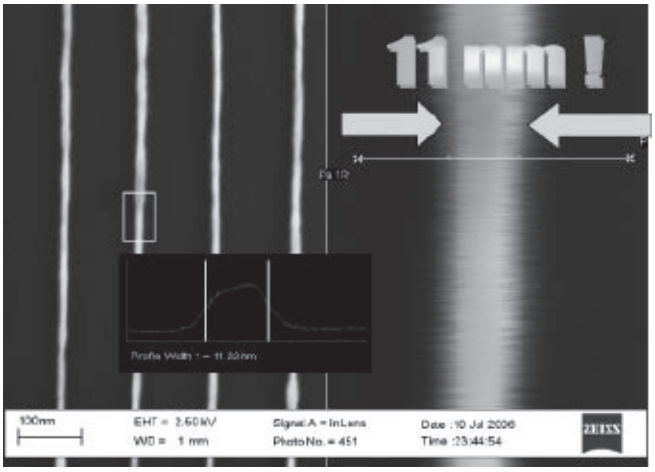

Figure 2, above: Zeiss SEM of an 11 nm line in HSQ using the JEOL electron beam lithographer.

Figure 3, below: Zeiss SEM image of 81 nm lines with 500 nm pitch.