Fabrication and Comparison of ZnO Thin Film Transistors with Various Gate Insulators

George Cramer
Electrical Engineering, The Cooper Union for the Advancement of Science and Art

NNIN REU Site: Michigan Nanofabrication Facility, University of Michigan
NNIN REU Principal Investigator: Jamie Phillips, EECS Department, The University of Michigan
NNIN REU Mentor: Jeffrey J. Siddiqui, EECS Department, The University of Michigan
Contact: cramer@cooper.edu, jphilli@engin.umich.edu

Abstract:

High electron mobility and visible transparency make ZnO thin film transistors (TFTs) an attractive alternative to amorphous silicon TFTs for use in flat panel displays. The insertion of a high-κ gate dielectric, $(Pb,Zr)TiO_3$ (PZT), into ZnO TFT structures was compared to SiO_2 and SiN_x gate dielectrics with the goal of improving switching characteristics and achieving lower operating voltages. ZnO thin films were deposited by pulsed laser deposition, PZT by a sol-gel process, and SiO_2 and SiN_x by PECVD. ZnO TFTs utilizing PZT insulators demonstrate significantly improved gate control, with some degradation in drain current.

Introduction:

A thin film transistor is a type of field-effect transistor that provides a common, inexpensive method of driving individual pixels in LCD and OLED displays. Increased drain currents resulting from high mobility are necessary for achieving high frame rates in high-resolution displays. Low deposition temperatures are essential for deposition on inexpensive, transparent substrates, such as glass and plastic. Zinc oxide is an ideal TFT semiconductor for these applications, having a higher mobility than amorphous silicon and lower deposition temperatures than polycrystalline silicon. Also, the high bandgap of ZnO (3.3eV) leads to a desirable level of transparency of the transistor itself. The use of high-κ dielectrics in TFTs is becoming increasingly necessary, as smaller transistors lead to unacceptable levels of gate leakage current. A high-κ PZT (κ ~ 100) dielectric replacement for SiO_2 (κ = 3.9) would serve to lower transistor operating voltages and allow the insulator thickness to be maintained, thus reducing gate leakage without sacrificing capacitance. This research compares the performance of ZnO TFT samples with three insulators: PZT, SiO_2, and SiN_x.

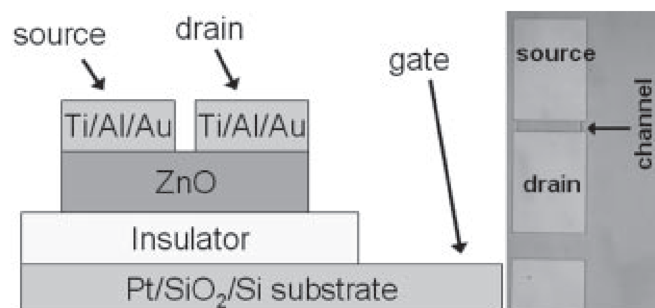


Figure 1: TFT schematic and SEM.

Experimental Procedure:

ZnO was deposited using pulsed laser deposition (PLD). In this process, the substrate was placed in a vacuum (10^{-6} Torr) and heated to 350°C. Under 30 mTorr O_2, the target was struck by a 248 nm KrF excimer laser pulsed at 350 mJ, 20 ns pulse width, and 6 Hz. The ZnO target was ablated, forming a plasma plume that deposited 80 nm of ZnO on the substrate. PZT was deposited using a sol gel process. PZT nanoparticles were spun onto the substrate in a colloidal suspension. A soft bake and rapid thermal anneal were used to evaporate the carrier solvent and to enhance crystallinity in the deposited thin film. A final thickness of 240 nm was measured. TFTs were fabricated on $Pt/SiO_2/Si$ substrates, which provided a common metal gate for all transistors (Figure 1). First, the insulators were deposited, PZT by the sol gel process, SiO_2 (240 nm) and SiN_x (150 nm) by PECVD at 400°C. Next, ZnO was deposited using the PLD technique.

Standard photolithography, metallization, liftoff, and wet chemical etching processes were used to form source/drain contacts and to access the Pt gate. The aspect ratio fabricated for these transistors was W/L = 113 μm/ 14 μm. A subsequent BHF etch was carried out to remove ZnO between each TFT, thus electrically isolating the devices. Current-voltage DC testing data was gathered using the Keithley 4200-SCS, while capacitance-voltage data was measured using a Boonton capacitance meter at 1MHz.

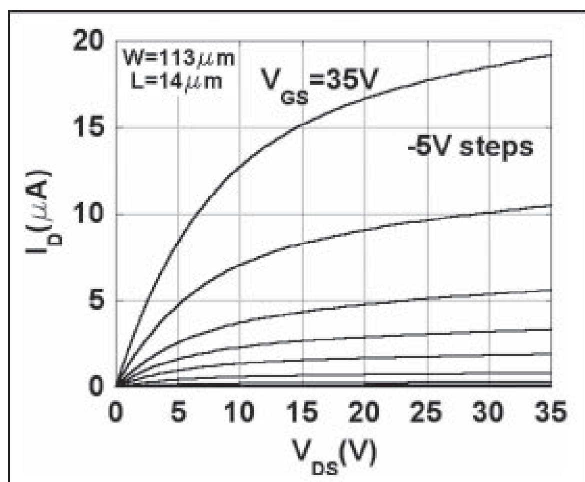
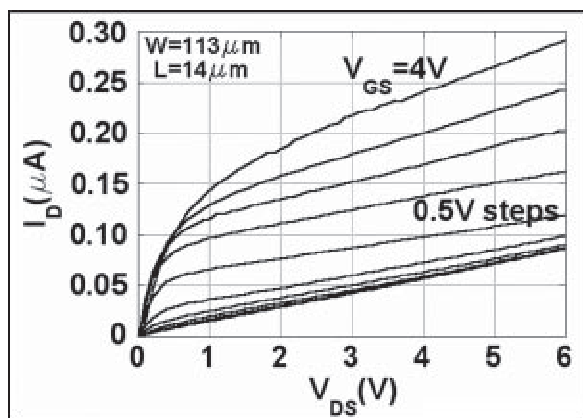


Figure 2, above: Silicon nitride TFT drain sweep.

Figure 3, below: PZT TFT drain sweep.



Results and Discussion:

The SiO_2 voltage sweep yielded results very similar to that of SiN_x, shown in Figure 2. Compared to both oxide and nitride, the PZT TFT works at much lower voltages, as shown in Figure 3. In addition, the PZT sample transitions from an "on" state to an "off" state with only a small change in gate voltage. This is evident by the small subthreshold slope given by Figure 4. These characteristics are related directly to the PZT sample's relatively high capacitance attributable to the high dielectric constant of the PZT material. The PZT sample also shows significantly lower drain current than either oxide or nitride. This undesired result coincides with the unexpectedly low value of mobility. Since the mobility is an intrinsic function of the ZnO channel between source and drain, this value should not change with different insulators. One possible cause would be a roughness of the PZT surface, which might hinder electron transport through the thin ZnO layer.

The ZnO mobility is very low even for the SiO_2 and SiN_x samples, given that a ZnO mobility of 27 $cm^2/V.s$ has been reported for similar ZnO deposition conditions [1]. The low ZnO mobility is likely a result of non-optimal ZnO PLD deposition conditions. The PZT TFTs began showing significant gate leakage current for gate voltages above 4V, possibly due to physical defects in the material associated with the sol gel process. Alternately, the low PZT bandgap (3.4 eV) relative to ZnO may not provide an adequate energy barrier to effectively impede current flow.

Future Work:

Adjust the PLD operating conditions to improve the ZnO crystal structure and maximize ZnO mobility. The resulting greater "on" current will improve the on/off current ratio. Also, attempt to reduce gate leakage, especially with PZT. Gate isolation helps to achieve this, but the current etch method can damage the device. Fabricating an independent gate for each transistor would provide an alternative to this etch. Gate leakage might also be reduced by investigating the use of thin, high-bandgap dielectric layers between ZnO and PZT. In addition, determine the level of physical uniformity of the PZT layer. A smoother PZT surface might reduce gate leakage and improve the effective channel mobility. Finally, attempt to reduce the "off" current by depositing a thinner layer of ZnO. This would increase the source/drain resistance and allow for easier depletion of charge in the semiconductor.

Acknowledgments:

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References:

[1] Fortunato, E; Barquinha, P; Pimentel, A; "Wide-bandgap high-mobility ZnO thin-film transistors produced at room temperature"; Applied Physics Letters, 85(13), 2541-2543 (2004).

	V_T	S (V/decade)	C_{ox} (F/cm^2)	I_{on}/I_{off}	μ ($cm^2/(V.s)$)
SiO_2	15V	24	2.54×10^{12}	75	0.30
SiN_x	11V	11	6.20×10^{12}	2×10^4	0.26
PZT	1V	0.66	2.25×10^{10}	7.2	0.025

Figure 4: Summary of results.