Fabrication of Sub-100 nm Structures Using Conventional Photolithography

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Abstract:

Although conventional photolithography has seen numerous applications within the microelectronics industry, its functional potential within nanotechnology has thus far been limited by its inability to produce pattern features effectively in the sub-micron range. However, through implementation of a novel technique in which microscale patterns are written onto the photoresist layers of a semiconducting wafer using conventional photolithography and then metals are angularly deposited through the pattern gaps, we have broken the conventional photolithography resolution limit. Through the course of research, pattern features less than 80 nm in size have effectively been produced.

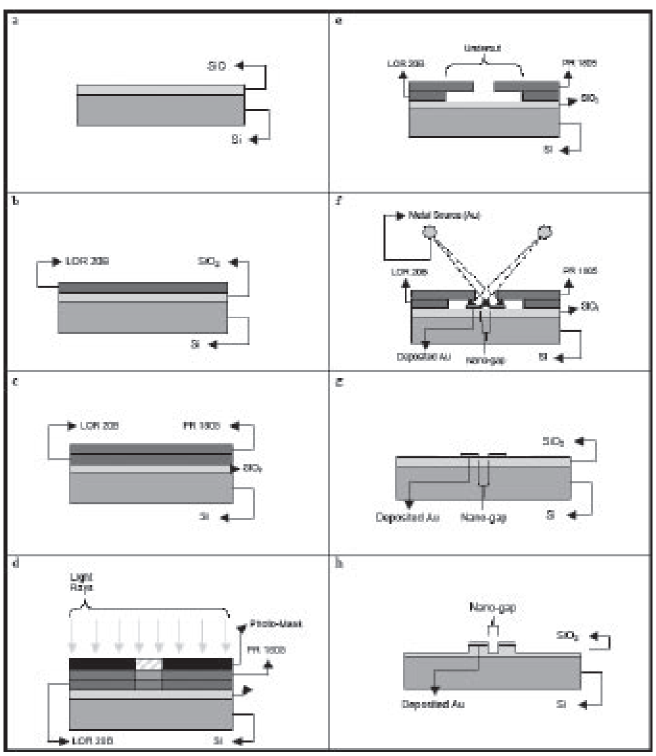

Figure 1: a) Diagram of initial Si/SiO_2 wafer, b) Coating with LOR 20B, c) Coating with PR 1805, d) Exposing with mask-aligner, e) Resist development, f) Gold deposition, g) Resist removal, h) Etching.

Materials & Process:

A detailed diagram of the fabrication is shown in Figure 1.

Spin Coating & Photolithography: Research was performed using silicon (Si) wafers with a layer of silicon dioxide (SiO_2) on the surface. The wafers were spin-coated with a layer of lift-off resist (LOR 20B), a thicker resist with a high dissolution rate during development. They were then spin-coated with photoresist (PR 1805). Conventional photolithography was used to expose the samples through a photomask with 1 μm pattern lines on it, and the samples were subsequently developed in order to transfer the pattern into the layers of photoresist. Because of the higher dissolution rate of the LOR 20B, an undercut was produced beneath the top photoresist layer, as shown in Figure 1e.

Thermal Evaporation: Samples were mounted into the upper stage of the thermal evaporator (Sharon) for the metal deposition. A thin layer of chromium (Cr) was first deposited to enhance subsequent gold adhesion. Two gold sources were used to deposit metal into the resist lines from two opposing angles. The deposition angle was varied by changing the spacing of two gold sources. In this experiment, the distance of the two gold sources was within 8.2 ± 0.5 cm.

Resist Removal: The resist layers were removed from the surface of the samples. This was accomplished by heating two beakers of MicroChem Remover PG to within a temperature of 60-70ºC and immersing the samples multiple times.

Reactive Ion Etching: To remove the thin layer of chromium within the nano-gap, samples were immersed in a wet etchant for 7 seconds. The samples were inserted into a reactive ion etcher (RIE, NEXX Inc.), which etched down the wafer surface around the gold pattern lines. A wet etchant was again used in order to remove any gold from the surface, leaving only the pattern etched into the wafer surface.

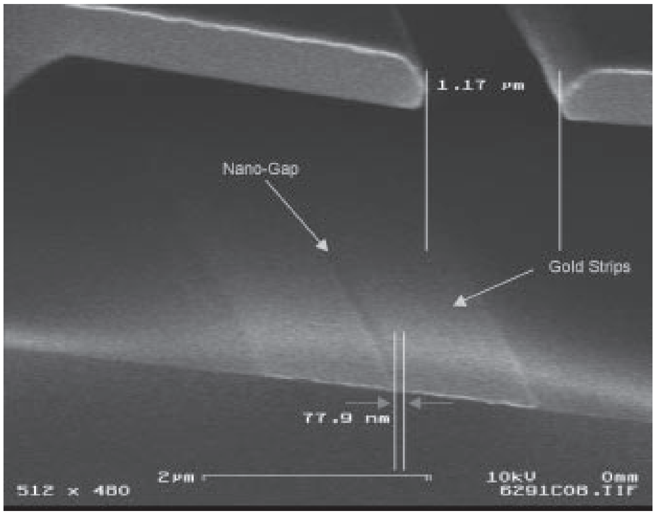

Figure 2: SEM: Nano-gap within LOR undercut showing a surface photoresist gap of 1.17 μm and a nano-gap of 77.9 nm.

Results & Discussion:

Optimizing Photolithography: During the photolithography process, the most significant determinant of pattern transference accuracy from mask to photoresist was the mask alignment exposure time. For the silicon samples coated with LOR 20B and photoresist S1805, an exposure time of 2.4 seconds was found to transfer the pattern with the highest accuracy and consistency while preventing excessive dissolution of the lift-off resist during development.

Manipulating Gap Size: Upon extensive testing and analysis, both the surface photoresist gap size and metal source spacing within the thermal evaporator were determined to have significant impact upon the produced nano-gap. The thinnest (1 μm) pattern gaps consistently yielded the smallest nano-gaps between deposited metal strips. It was also found that the nano-gap width could be controlled by varying the spacing between the two metal sources within the thermal evaporator. In Figure 2, by implementing a source spacing of 8.4 cm, a nano-gap of approximately 78 nm was achieved and imaged using a scanning electron microscope (SEM).

The Final Product: Upon measurement, the width of the nano-gap was found to be 71.6 nm (Figure 3), approximately 4 nm thinner than when the gap was imaged prior to reactive ion etching. A possible cause of this variance was that because of the angular deposition of the gold, the line edges may have lain at an angle to the surface of the wafer, therefore tapering inwards (towards center of nano-gap) near the surface and further reducing the width of the etched area. The height of the gap was recorded at 52.2 nm, a value which for the purposes of this research was satisfactory but could potentially be increased by longer RIE etching.

Conclusions and Recommendations:

Through the application of this novel cross-metal deposition into a lift-off resist undercut, the consistently successful fabrication of a nano-gap of less than 80 nm was evaluated. It was also shown that simply varying the metal source spacing could lead to a significant change in gap size using this technique. Therefore, the pattern feature size is no longer limited by diffraction as it has previously been in conventional photolithography.

Upon further research and refinement of testing conditions, this technique has the potential to open new doors for conventional photolithography. Adjusting exposure time and metal source spacing allows the process to be customized for applications requiring nanoscale features of specific sizes. Through slight manipulation of the reactive ion etching recipe, the produced wafer may be delicately refined for actual semiconductor device implementation. Additionally, creating a poly-dimethylsiloxane (PDMS) stamp of features created using our technique would allow for fast and effective reproduction of patterned features.

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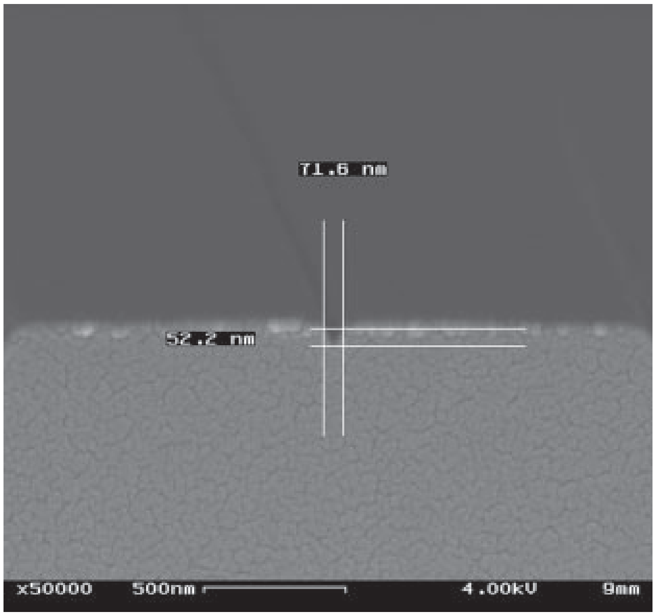

Figure 3: SEM: Cross-sectional view nano-gap width = 71.6 nm, height = 52.2 nm.

PROCESS & CHARACTERIZATION