Processing for Enabling Ultra-Fast Modulators on Chip

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Albert Kamanzi
Physics, University of Massachusetts at Boston

NNIN REU Site: Cornell NanoScale Science & Technology Facility, Cornell University
NNIN REU Principal Investigator: Prof. Michal Lipson, School of Electrical and Computer Engineering, Cornell University
NNIN REU Mentor: Carl Poitras, School of Electrical and Computer Engineering, Cornell University
Contact: alkamuk@yahoo.co.uk, ML292@cornell.edu, cbp8@cornell.edu

Abstract:

In order for ultra-fast electro-optic modulators to perform faster [1], low resistance ohmic contacts are required. Several methods have been developed to achieve these contacts. For silicon chips, transition metals are made to react with the silicon at the contact points, forming silicides. The most used silicide is $TiSi_2$ due to its low resistivity. For very thin layers (nanoscale) of silicon on insulator (SOI), this technology faces challenges with the difficulty to obtain $TiSi_2$, with high resistance TiSi being formed instead. We focus on forming contacts using both titanium and nickel for silicidation. The metal deposition and annealing times are carefully controlled and varied to determine the best contacts on thin silicon layers of 50, 100 and 150 nm.

Introduction:

The electro-optic modulator under consideration is made up of waveguides and a p-i-n diode, as shown in Figure 1. The diode must be of minimum thickness so as to not affect the light propagating in the waveguides.

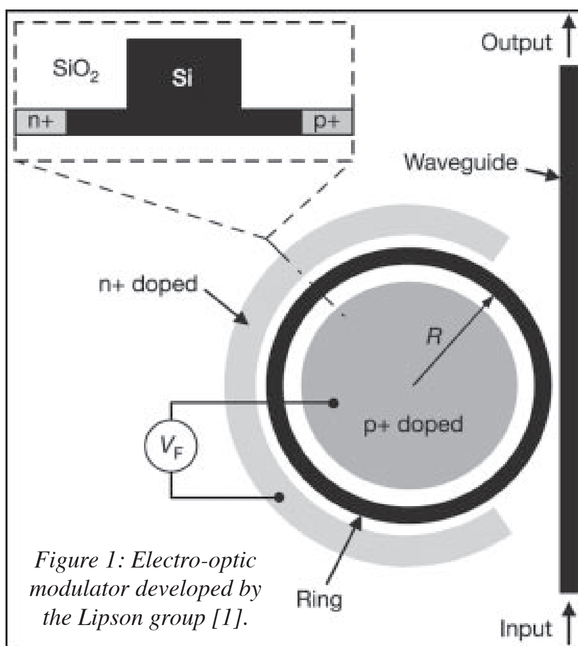

Figure 1: Electro-optic modulator developed by the Lipson group [1].

Formation of metal contacts then presents a difficulty because it involves the formation of silicides on thin silicon, around 50 nm. The silicidation is an important process because it allows for a gradual change in chemical potentials from the silicon to the top metal pads, and therefore requires investigation.

In this project, $TiSi_2$ and NiSi are separately investigated and are formed on thin SOI. Titanium is used because $TiSi_2$ has low resistivity [2]. Also Ti is very effective at reducing native oxides in contacts. But a major drawback is that it can form another higher resistivity silicide, TiSi. By carefully monitoring the annealing process and the amount of metal used, these two silicides can be controlled. This is the main aim of the project. With nickel, only one silicide is formed (NiSi). The formation of NiSi consumes less silicon than in the $TiSi_2$ process, and is therefore more appropriate for use with thin layers of silicon.

Experimental Procedure:

The devices were built on three SOI wafers with 50, 100 and 150 nm of silicon respectively. The various devices included resistors, diodes and sheet and contact resistance test structures (including structures which use the transfer length method (TLM). See Figure 2).

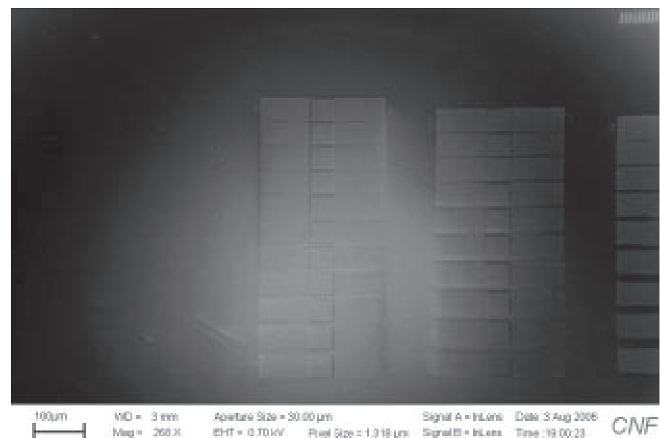

Figure 2: TLMs that were used to measure resistance as a function of separation distance.

Photolithography was used to define the layers onto the wafers using the GCA Autostep 200 stepper. The active regions were implanted with boron (n+) and arsenic (p+) to concentrations of about 10^{19} cm^{-3}.

A 1 μm layer of silicon dioxide was then deposited onto the wafers by plasma-enhanced chemical vapor deposition. The contacts were then defined also using the Autostep, followed by a SiO_2 etch using the Plasmatherm 72 fluorine etcher. The contact metal (Ti or Ni) was then evaporated onto the wafers after they underwent a quick HF dip. The annealing step followed using a rapid thermal anneal (RTA) tool. Chips with Ti were annealed at 400°C for 180s, then at 650°C for 120s and then at 800°C for 30s. As for Ni, the anneal was done at 500°C for 30s. A last photolithography step defined the metal pads (for laboratory testing), and Al was evaporated.

Results And Conclusions:

The TLMs were used for measuring the contact resistance of the silicides. This technique allows for the measurement of contact resistance between neighboring pads that are separated by a gradually increasing distance, using a 4-probe setup. The contact resistance is extrapolated for a null separation distance (see Fig. 3).

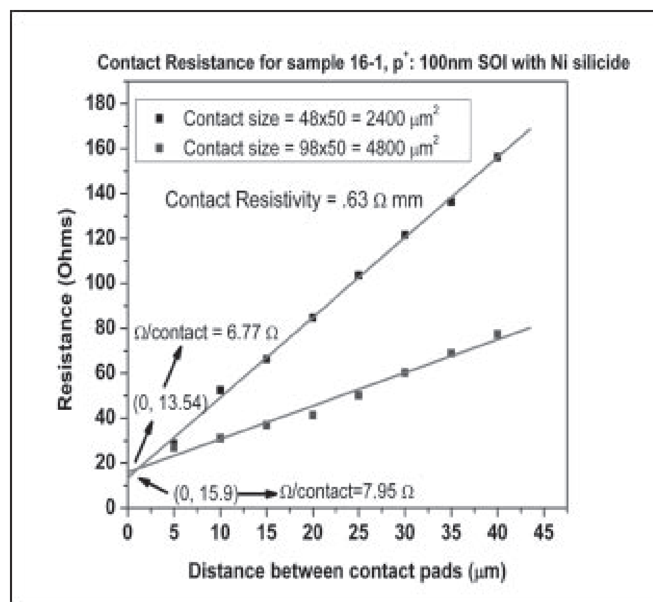

Figure 3: Example of measured resistance as a function of distance between measuring probes for a given TLM.

Table 1 shows the extrapolated contact resistance for chips with NiSi. The values are much lower than for the Ti contacts, where measurements were about 10-20 times higher. Ni definitely offered the lowest contact resistance. It is possible that the Ti contacts did not form a good silicide.

Future Works:

Ni appears to offer the lowest contact resistance for this type of technology. It does require a low temperature anneal which was performed using an RTA outside of the clean room. If Ti is still to be considered for the silicide, the use of this outside tool should be considered since it is reliable at low temperatures—as compared to the RTA tool in the clean room which is accurate only at temperatures above 600°C. Several of the required anneals are below this temperature.

A recipe which was expected to give better results for titanium contacts was not tested because of time limitation. This would involve depositing titanium at a thickness of only 20% of that of the silicon layer. Using less Ti could prove beneficial because when excess Ti is present, it reacts with the formed $TiSi_2$ giving TiSi. Another important step would be to anneal the titanium chips at temperatures above 850°C. At this temperature, $TiSi_2$ converts its phase from C49 to a lower resistivity phase, C54 [3].

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References:

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50 nm layer	100 nm layer
1.0 Ωmm (n+ doped)	0.3 Ωmm (n+ doped)
1.9 Ωmm (p+ doped)	0.6 Ωmm (p+ doped)

Table 1. Contact resistance for the NiSi contacts.