Construction of a Modulated Potential Superlattice

Phillip Meyerhofer

Department of Physics, Saint Vincent College

NNIN REU Site: Penn State Nanofabrication Laboratory, The Pennsylvania State University, University Park, PA

NNIN REU Principal Investigator: Jun Zhu, Department of Physics, The Pennsylvania State University

NNIN REU Mentors: Jing Li and Ke Zou, Department of Physics, The Pennsylvania State University

Contact: phillip.meyerhofer@email.stvincent.edu, jzhu82@gmail.com, jingli.psu@gmail.com, sky22124@gmail.com

Abstract:

A superlattice is a periodic structure composed of at least two different materials and may be used to change the band structure of a semiconductor. We studied the construction of a periodically modulated potential superlattice (with a 60-200 nm period) that we predicted would allow microscale manipulation of electron transport properties in graphene. Using electron beam lithography and reactive ion etching followed by metal deposition, we constructed complete 200 nm and 140 nm period superlattices. We also pushed the size limitations of our process to lay ground work for 100 nm and 60 nm period superlattices.

Introduction:

The study of graphene's electrical properties has been and continues to be a popular field of research. Our particular interest was in the prediction that by applying the correct periodic potential, electrons could be made to move freely in graphene without scattering. We investigated the parameters necessary to produce such a potential.

Because the mean free path of electrons in graphene is on the order of tens to hundreds of nanometers, the periodicity of the potential must be around a few tens of nanometers to affect the movement of electrons. The way we chose to attempt to create this potential was by constructing a superlattice (see Figure 1). This superlattice alternated gold with silicon oxide. Applying a voltage to the gold created a potential and the spaces of insolating silicon oxide limited the size of the potential. We chose to pursue this process by using a top down approach.

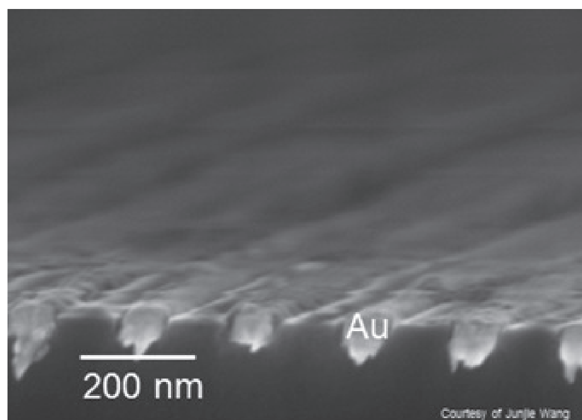

Figure 1: Superlattice.

Methods:

We began with a typical silicon wafer covered in 290 nm of thermally grown silicon oxide. We needed to etch the surface to create a space that would be filled with gold. The patterning of the surface prior to etching was done using electron beam lithography. We chose the resist Zep 520a because of its resistance to etching and its resolution.

One-hundred to about fifty nanometer trenches alternating with same-sized spaces were easily achieved using a Vistec 5200 and a standard develop procedure of 180 seconds in n-amyl acetate, followed by thirty seconds in 8:1 MIBK to IPA, and another thirty seconds in straight IPA to stop the develop process. However, as we approached the 30 nm mark out, the electron beam dose went straight from under-exposed to over-exposed (see Figures 2 and 3). This appeared to be because of proximity effect damage on the adjacent resist walls.

When the electrons were shot at the resist during exposure they broke the polymer chains and at the same time excited secondary electrons. Most of these secondary electrons were much less energetic and, especially at high accelerating voltages (we used 100kV), did not travel far laterally — only a few nanometers. These secondary electrons thus contributed mostly to exposing the pattern in the resist. There were, however, some fast secondary electrons (possibly caused by backscattering) that traveled much further and caused infidelity in the pattern.

This collateral damage became increasingly important as the patterns being written became smaller and closer together. Because of this, as our structures got closer and closer together, the damage to the thin walls of the trenches became catastrophic to the point where our somewhat harsh develop procedure removed not only the parts that we wanted to expose, but also large parts of the adjacent resist that had been damaged by stray electrons.

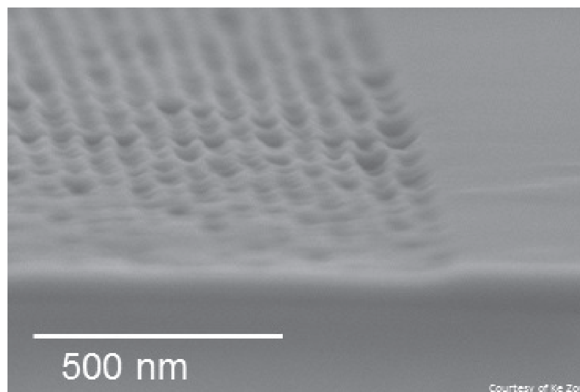

Figure 2: Underexposed line space pattern.

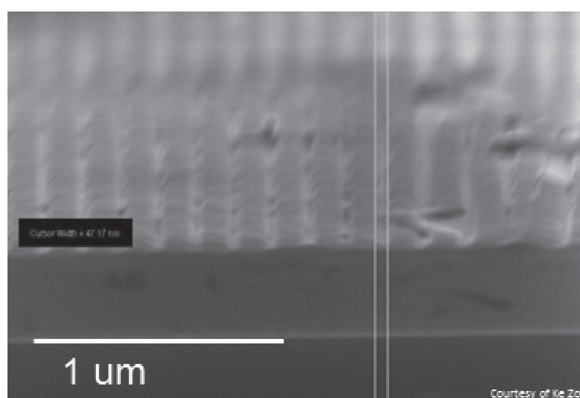

Figure 3: Overexposed line space pattern.

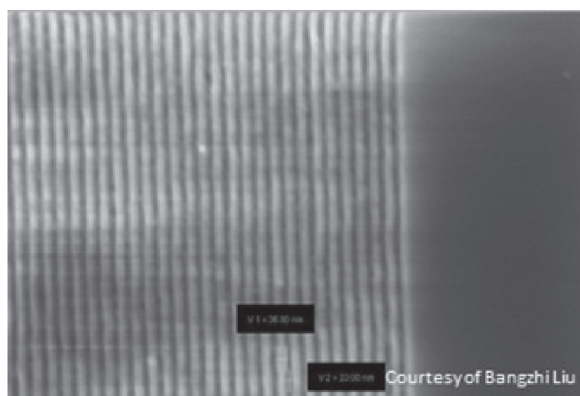

Figure 4: Cold develop lines.

In order to make this process work, we needed a develop process that was gentle enough to leave the damaged resist, while still removing the exposed resist. A shorter develop time (thirty seconds to a minute and a half) was attempted, but without success. The shorter develop time had to be combined with a colder develop temperature. Because of the kinetics of the removal process, it was possible to make the developer cool enough (down to ~ 4°C) that it removed the normally exposed resist while leaving intact the damaged/partially exposed sides (see Figure 4). In order to make this work, it was necessary to increase the dose to a much higher level.

Success using a similar technique was achieved by Mr. Frazier Mork, as reported at the 2012 NNIN REU Convocation [1]. Using a cold develop and a 30 nm thick resist, as well as dose correction, his group achieved ~ 20 nm line spacing.

Conclusions:

Using our process, we believe that it would be difficult to decrease the resist thickness any more than our 140 nm — which we achieved using 1:1 ratio anisole to zep — because the pattern must then survive etching. We etched with a combination of CF_4 and CHF_3. Metal deposition may be done with regular electron beam evaporation, and finally for lift off, we used warm remover PG with sonication. (Acetone would also work though it is less aggressive.) We achieved a successful superlattice (see Figure 1) that was too large for experimentation, although it did demonstrate the method. Using the cold develop method, we demonstrated the technique's viability for use in smaller structures.

Acknowledgements:

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References:

[1] "Substrate Conformal Imprint Lithography"; F. Mork, 2012 NNIN REU Research Accomplishments, pgs. 216-217.