Silicon Nanowires for Optical Light Trapping in Solar Cells

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Introduction:

The advanced development of the semiconductor industry has placed crystalline silicon solar cells at the forefront of solar cell research. Currently, crystalline silicon solar cells (c:Si SCs) average around 20% efficiency in the conversion of sunlight into electricity [1]. Control of the surface morphology of solar cells is key to boosting the conversion efficiency beyond the current average through the reduction of reflectance and the enhancement of electrical performance. Inexpensive surface texturing is commonly used to minimize reflection losses; however, this method is dependent on the refractive index of the semiconductor and quickly reaches a maximum. Nanowires with sub-wavelength dimensions (~ 100 nm) offer great potential for decreasing reflectance beyond the bulk limit. These attributes are shared with other sub-wavelength scaled features, but nanowires offer the unique ability for the separation of light absorption and carrier transport through the confinement of electrons in two dimensions [2].

The approach used in this experiment to fabricate nanowires on silicon devices allowed for well-controlled nanowire structures. Using electron beam lithography (EBL) and deep reactive ion etching (DRIE), highly ordered nanowire patterns were produced on doped c:Si wafers. With additional processing, the resulting silicon nanowire solar cells were characterized optically and electrically. A schematic diagram of the finalized device structure is shown in Figure 1.

Experimental Procedure:

Nanowires were fabricated on back-side junction c:Si SCs with amorphous silicon (a:Si) passivation and aluminum contacts. To begin the fabrication process, a backside junction was formed on p-type c:Si wafers. This was done using backside diffusion of phosphorus at 1000°C for one hour. A drive in stage was performed after diffusion for seven hours at 1000°C. The front side of the wafers was coated with PMMA photoresist and patterned using EBL, forming exposed circular areas of 70 nm and 100 nm diameter after development. To form a hard mask for etching, 30 nm of silicon dioxide (SiO_2) was deposited with electron-beam evaporation, leaving a grid pattern of SiO_2 islands with 700 nm spacing.

DRIE etching was done using a Surface Technology Systems inductively coupled plasma (STS ICP) system. Highly anisotropic nanowires of diameters 70 nm and 100 nm, and a height of around 600 nm, were formed using the Bosch process (shown in Figure 2), which consists of alternating cycles of etchant sulfur hexafluoride (SF_6) and deposition polymer octaflourocyclobutane (C_4F_8). This method inherently creates scalloping on the sides of the nanowires.

A passivation layer was deposited using PECVD, consisting of a 10 nm intrinsic layer of a:Si, followed by 30 nm of p^+ a:Si. This increased the diameters of the nanowires to 150 nm and 180 nm. Electron-beam evaporation was used to deposit 200 nm of aluminum (Al) on the front and back sides of the wafer. A shadow mask was aligned on

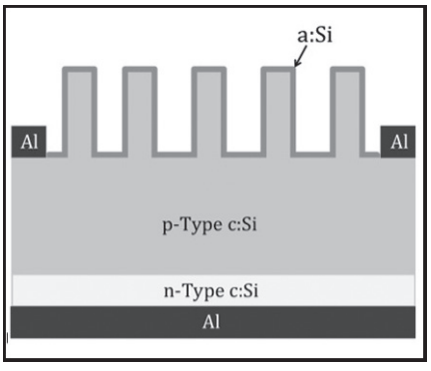


Figure 1, above: Schematic representation of finalized device (not to scale).

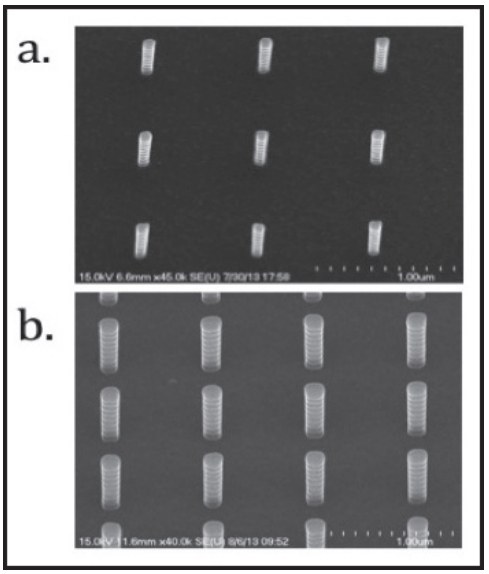
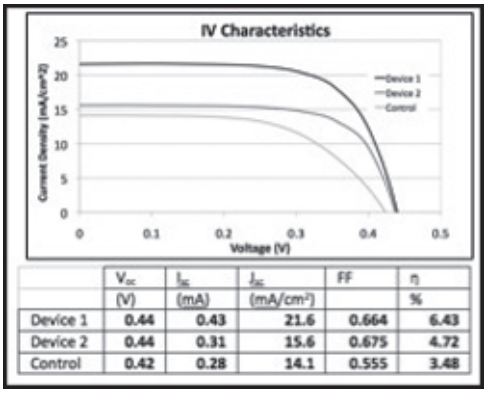


Figure 2, right: SEM images of nanowire (a) after etching and (b) after a:Si deposition.



	V_{oc} (V)	I_{sc} (mA)	J_{sc} (mA/cm²)	FF	η %
Device 1	0.44	0.43	21.6	0.664	6.43
Device 2	0.44	0.31	15.6	0.675	4.72
Control	0.42	0.28	14.1	0.555	3.48

Figure 3: (a) IV characteristics of nanowire and control devices and (b) tabulated data from IV characteristics.

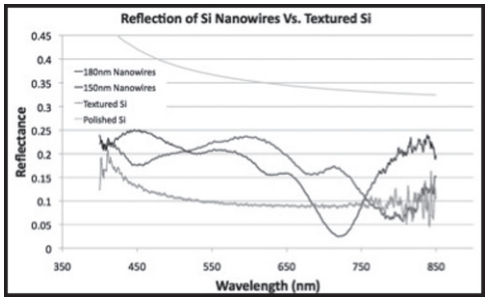


Figure 4: Reflectance measurements of 180 nm and 150 nm devices along with planar and textured Si.

150 nm diameter nanowires and at 800 nm wavelength for 180 nm diameter nanowires. The nanowire structures showed higher absorption at the observed peaks than textured Si. A red shift in absorption peaks with increased diameter shows tunability of the absorption peak through the diameter of the nanowires. Similar results were observed in indium arsenide and indium phosphide nanowires by Kupec [3].

the front side of the wafer during deposition to avoid contact with the nanowires. Finally the wafers were placed in an oven at 300°C for 20 minutes to allow the Al to diffuse through the passivation layer without compromising the amorphous nature of the layer.

Results and Conclusions:

Figure 3 shows the current-voltage (IV) characteristics of the nanowire devices under AM1.5 illumination. Under these conditions, the best device showed an open circuit voltage (V_{oc}) of 0.44 V, a short circuit current density (J_{sc}) of 21.6 mA/cm^2, a fill factor (FF) of 0.664, and an efficiency (η) of 6.43%. The control device used was a planar c:Si device located on the same wafer as the nanowire devices. The control device showed a V_{oc} of 0.42 V, J_{sc} of 14.1 mA/cm^2, FF of 0.555, and η of 3.48%. Light trapping in the nanowire structures increased the absorption of incident photons over the planar device.

Reflectance measurements were taken of 150 nm and 180 nm diameter nanowire patterns, and textured Si using a Filmetrics F40 microscope attachment, and a reference was used for planar Si. The results are shown in Figure 4. Nanowire devices showed higher absorption than planar Si, but textured Si showed a higher total absorption than the nanowire devices. Absorption peaks were observed at 700 nm wavelength for

Future Work:

Further research is needed to optimize the fabrication process so that control devices perform at a higher efficiency. Studies on the effects of nanowire diameter, spacing, and structure on absorbance must be performed to allow for optimization of nanowire structures. Eventual applications may focus on radial p-n junction nanowires and nanowire thin film devices using similar fabrication methods.

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References:

[1] Garnett, Erik, and Peidong Yang. "Light Trapping in Silicon Nanowire Solar Cells." NanoLetters 10 (2010): 1082. 28 Jan. 2010.

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