Interlayer Dielectric and Interconnect for Heterointegration

Julie Miller

Chemical Engineering, The Pennsylvania State University

NNIN REU Site: Lurie Nanofabrication Facility, University of Michigan, Ann Arbor, MI

NNIN REU Principal Investigator: Prof. Rebecca L. Peterson, Electrical Engineering and Computer Science, University of Michigan

NNIN REU Mentor: Bradley Frost, Electrical Engineering and Computer Science, University of Michigan

Contact: jam6451@psu.edu, blpeters@umich.edu, bfrost@umich.edu

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Introduction:

In order to vertically integrate heterogeneous electrical devices, compatible processes for interlayer dielectrics and metal interconnects are needed. The focus of this project was to study silicon dioxide (SiO_2) as an interlayer dielectric for heterointegration of two process technologies. The first step of this project was to develop and characterize a deposition process for high quality plasma enhanced chemical vapor deposition (PECVD) SiO_2 film by fabricating capacitors and testing film electrical characteristics. Once the dielectric was assessed to be viable, via etch hole and metal interconnect technologies were developed and characterized. Test structures were made to verify the electrical connection between the top contact of the bottom device and the bottom electrode of the top device. These test samples were followed by fabrication of the heterogeneously integrated devices. The ability to reliably integrate heterogeneous devices will enable new applications.

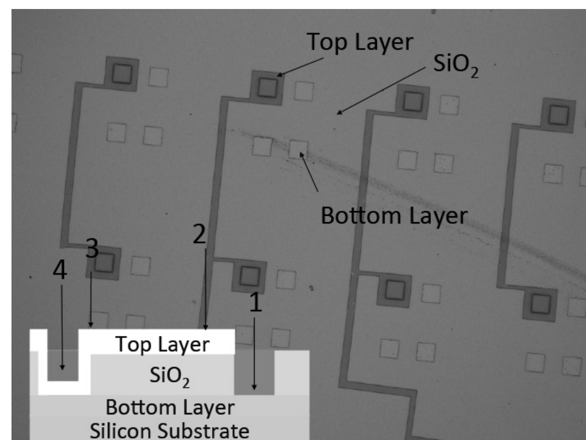

Figure 1: Structures for testing side wall coating of top metal. Numbers on the inset cross-section indicate test probe points for current-voltage measurements of Figure 3.

Experimental Procedure:

First metal-insulator-metal (MIM) capacitors were fabricated to identify a suitable dielectric film and to develop a deposition technique that would have a limited effect on previously fabricated devices existing on the substrate. Using PECVD, four different films were deposited on four 100 mm silicon wafers. Two were deposited at 200°C with thicknesses of 200 nm and 500 nm. These thicknesses were also deposited at 380°C. Tungsten was deposited using the LAB 18-02 PVD sputter tool and a shadow mask to form the top capacitor plates. Capacitance-voltage (C-V) and current-voltage (I-V) measurements were taken to determine film properties.

Once the 380°C film was determined to be a suitable dielectric, the etch rate of the film was characterized. The LAM 9400 was used for reactive ion etching (RIE) of SiO_2 with a power of 500W and gas flows of 8 sccm of SF_6, 50 sccm of C_4F_8, 50 sccm of He, and 50 sccm of Ar.

Next, test samples were fabricated to test the metal interconnects. A 100 nm film of aluminum (Al) was deposited on glass substrates followed by deposition of 1 μm SiO_2. The SiO_2 was etched to create vias to the Al layer. These etch holes were covered with top metal pads as shown in Figure 1. I-V measurements were performed to determine the resistance of the metal interconnect. Finally, the optimized SiO_2 film was used as a passivation layer between two sets of transistors.

Results:

From the C-V data measured on the MIM capacitors, the experimental dielectric constants of the SiO_2 films were calculated. Its value for the 380°C film was very close to the ideal value of 3.9 [1]. This indicated that the film was dense and of a fairly high quality. I-V measurements of leakage current

were also taken, and are shown in Figure 2. The 380°C film maintained a low leakage current throughout the sweep, indicating its functionality as an insulator, while the 200°C film had significantly higher leakage current. While the 200°C oxide would be preferred for low temperature processing, the low leakage of the 380°C film makes it a better choice for heterointegration [2].

As shown in Figure 3, the resistance present between the metal pad and the side of the etch hole was approximately 23.3Ω. The resistance between the top metal pad and the bottom of the etch hole was 87.9Ω — meaning that the resistance of the side wall was about 65Ω. This large increase in resistance was due to the method used to cover the side walls of the etch holes. The sputtered metal was thin relative to the dielectric layer and thus only a very thin coating was present on the side walls.

The resistance between the top metal pad and the bottom aluminum surface was measured to be 117Ω. Thus the resistance added by the contact between the two metals was only about 20Ω. This indicates both that there was a good connection between the two metals and that there was no SiO_2 at the bottom of the etch holes. Both of these are important requirements for heterointegration of two devices.

Using the SiO_2 passivation layer, two layers of functioning transistors were fabricated. Devices in the first layer maintained their functionality even after top device fabrication, and the top devices displayed switching behavior. Figure 4 displays the results of I-V sweeps on both a bottom and a top layer transistor.

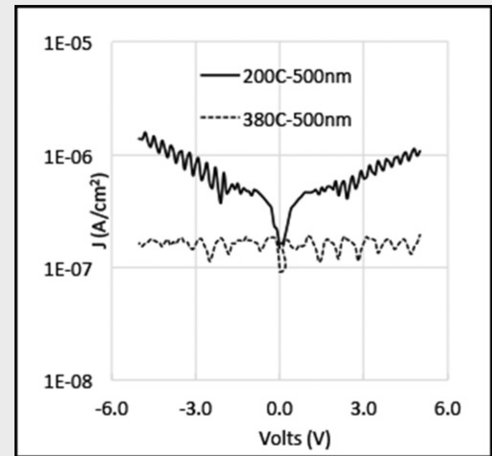

Figure 2: Average leakage current vs. voltage of 0.003 cm^2 SiO_2 MIM capacitors.

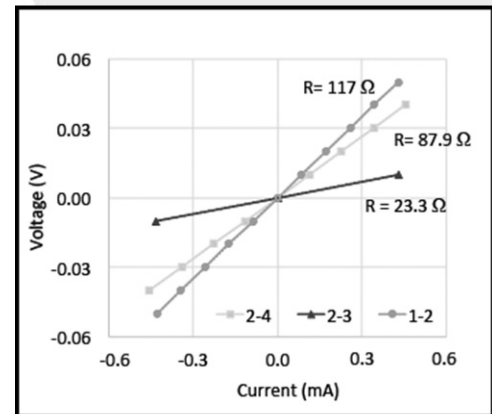

Figure 3: Resistance of metal interconnect test structures used to determine the quality of the metal vias.

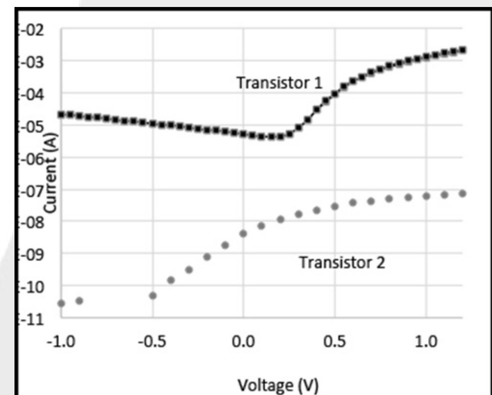

Figure 4: Measured drain current vs. gate voltage for one top layer and one bottom layer transistor. Both devices show field-effect behavior, indicating the successful heterointegration.

Conclusion and Future Work:

This experiment showed that SiO_2 is a suitable interlayer dielectric for the integration of two process technologies. A plasma etch was used to create openings in the SiO_2 down to the metal interconnect of the bottom device. Test samples showed that a thin metal layer could establish a reliable electrical connection through these etch holes to provide suitable vias for integrating top devices. Future work could be done to further improve the sidewall coverage and reduce via resistance. Two layers of functioning transistors were fabricated using a SiO_2 interlayer dielectric.

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References:

[1] Robertson, J. High Dielectric Constant Oxides. Eur. Phys. J. Appl. Phys., 2004, (28), 265-291.

[2] Ko, C.T., and Chen, K.N. Low Temperature Bonding Technology for 3D Integration. Microelectronics Reliablity, 2012, (52), 302-311.