Vanishing Programmable Resources: Design, Materials, and Characterization

Mary E. Alsobrooks
Chemical Engineering, the University of Alabama

NNIN REU Site: Institute for Electronics and Nanotechnology, Georgia Institute of Technology, Atlanta, GA
NNIN Principal Investigator: Dr. Paul A. Kohl, Chemical and Biomolecular Engineering, Georgia Institute of Technology
NNIN Mentor: Jared M. Schwartz, Chemical and Biomolecular Engineering, Georgia Institute of Technology
Contact:mealosbrooks@crimson.ua.edu, paul.kohl@chbe.gatech.edu, jschwartz38@gatech.edu

Abstract and Introduction:
Printed wiring boards (PWBs) act as the mechanical structure supporting the electronic connections between the different functional components in microelectronic devices. Stable materials are generally desired so that long mission life can be achieved, however, there is growing interest in self-decomposing materials because of environmental concerns. Sustainability requires an effective way to dispose of the multitude of PWBs currently in use. This has prompted the development of PWBs that can be triggered to disappear after a time-independent, fully-functional life span.

For this project, an optically-triggered disappearance mechanism was explored. UV-sensitive polymers, poly(phthalaldehyde-co-butyraldehyde) and poly(dihydroxy-tetrahydro naphthalene), Figure 1, were characterized using nanoindentation. Four-point probe analysis was used to analyze composite films that contained 3 µm dendritic copper nanoparticles; the addition of copper provided the conductive portion of the PWB. Composite films were also made using photo-acid generator (PAG), an iodonium salt, to improve the optical-trigger. Layered-films, comprised of stacked composite films, were analyzed using exposure techniques. This method of construction was used to test the permeability of the stacked films.

Experimental Procedure:
In order to test the different films, formulations were made following the same basic procedure: the polymer solids, solvent, and additional materials were combined in a vial and vortexed/sonicated. See Table A for the list of formulations made, including the use, basis, solvent, and soft-bake/cure procedure for each. The optimum loading for metal nanoparticles is 70-80 vol% [1], so 75 vol% was chosen as our loading. The copper used was cleaned in an acid bath and stored under PGMEA. All formulations containing PAG were made and worked with in the dark. Films were made using a doctor-blading technique.

Nanoindentation was done to find the reduced Young's modulus and hardness of the polymers. A 10-second load, 10-second hold, 4-second unload function was used, and a 9-point matrix of decreasing force from 650 µN to 50 µN was used to collect data points. An area function was created using polycarbonate as a standard. Four-point probe analysis was done on the copper and polymer films to measure sheet resistance to be used to calculate conductivity.

The layered-films were exposed to a dose of UV-light that we knew would activate all of the PAG to determine if the copper/polymer film was permeable to the acid generated from the top film. The layered-films were exposed to a dosage of 10000 mJ/cm², and before, immediately after, and every hour after the exposure, the resistance of the copper/polymer film was tested using a multimeter.

<table>
<thead>
<tr>
<th>Solids</th>
<th>Solvent</th>
<th>Basis</th>
<th>Soft-Bake/Cure</th>
<th>Use</th>
</tr>
</thead>
<tbody>
<tr>
<td>p(PHA-co-BA)</td>
<td>GBL</td>
<td>30-40 wt% polymer</td>
<td>100°C for 5 min</td>
<td>nanoindentation</td>
</tr>
<tr>
<td>p(DHTN)</td>
<td>GBL</td>
<td>30-40 wt% polymer</td>
<td>100°C for 5 min</td>
<td>nanoindentation</td>
</tr>
<tr>
<td>Cu/polymer</td>
<td>PGMEA</td>
<td>75 vol% Cu</td>
<td>100°C for 5 min</td>
<td>four-point probe</td>
</tr>
<tr>
<td>Cu/polymer</td>
<td>THF</td>
<td>75 vol% Cu</td>
<td>air cure for 10 min</td>
<td>layered-films</td>
</tr>
<tr>
<td>PAG/polymer</td>
<td>THF</td>
<td>30 wt% polymer/10 phr PAG</td>
<td>air cure for 10 min</td>
<td>layered-films</td>
</tr>
</tbody>
</table>

Table A: Formulations.
Results and Conclusions:

Nanoindentation testing of p(PHA-co-BA) and p(DHTN) gave reduced Young’s moduli of 4.56 GPA and 0.055 GPA, and hardness readings of 270 MPA and 3.1 MPA, respectively. We compared the polymers to ideal values represented by FR4: a reduced modulus of 24 GPA and a hardness of 200 MPA. FR4 is a fully cross-linked, epoxy board with fiberglass matrix and is meant to be rigid and long-lasting. The p(PHA-co-BA) values are promising, especially the hardness because it is above the ideal. The modulus and hardness of p(DHTN) are far enough below the ideal values. This polymer did display tacky qualities, both qualitatively through observation and quantitatively by the unloading function displayed in its indentation profile. The low values dismissed p(DHTN) as a possible bulk material for the PWB, but the adhesive quality it has made it potentially useful for areas like conductive contacts connecting devices to the board.

Four-point probe analysis resulted in a conductivity of $4.5 \times 10^3 \, \Omega^{-1} \cdot m^{-1}$ for a 75 vol% Cu film. This is several magnitudes below the bulk copper value of $4.9 \times 10^7 \, \Omega^{-1} \cdot m^{-1}$ due to the nature of nanoparticles and the resulting oxidation issues. These were combatted using cleaning methods on the copper and by using the layered-films as a construction technique. Copper nanoparticles are still effective for the conductive portions of the PWB even with a lower conductivity in the polymer matrix.

Initially, we attempted to create formulations that included the polymer, copper, and PAG in solvent. These formulations were not successful because the copper and PAG interacted in a way that depolymerized the matrix and oxidized the copper before being triggered. A new construction technique, layered-films, Figure 2, was considered to combat the oxidation/depolymerization issue. Layered-films showed an increase in the resistance of the copper/polymer film after exposure. The resistance increased several magnitudes over the course of three hours, from 2 MΩ to 200 MΩ. This showed that the acid was diffusing through the copper paste and depolymerizing the polymer matrix after triggering, and that layered-films would be an applicable construction technique.

Future Work:

In order to improve upon the material used in the transient PWBs, several areas may be investigated or expanded upon. An investigation of newly synthesized polymers with faster rates of depolymerization and vapor evolution will be helpful for improving the bulk and conductive matrices. Expanded testing of the adhesion strength of p(DHTN) should be done to determine the full extent of use for the material. The ultimate end goal of the future work is to fabricate a fully functional PWB using the explored methods and materials. This PWB will need conductivity testing to ensure electrical connections are functional before triggering and non-functional after. Devices can then be added to the PWB to create a multi-functioning sensor.

Acknowledgments:

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References:

Electrostatic Gating of MBE-Grown NdTiO₃ Thin Films

Emilie Benson  
Physics and Chemistry, Gustavus Adolphus College

NNIN REU Site: Minnesota Nano Center, University of Minnesota-Twin Cities, Minneapolis, MN  
NNIN REU Principal Investigator: Professor Bharat Jalan, Department of Chemical Engineering and Materials Science, University of Minnesota  
NNIN REU Mentor: Andrew Xu, Department of Chemical Engineering and Materials Science, University of Minnesota  
Contact: ebenson@gustavus.edu, bjalan@umn.edu, andrewxu@umn.edu

Abstract:
With the emergence of ionic gel gating in an electric double-layer transistor, materials that could not be easily chemically doped, or had significant structural changes upon being doped, can now be examined. Neodymium titanium oxide (NdTiO₃ or NTO) is a Mott-Hubbard antiferromagnetic insulator, with the insulating state being sensitive to doping and chemical distortions. This experiment explores the use of ionic gel gating to investigate the insulator-to-metal transition in NTO thin films using electrostatic doping. Single crystalline, epitaxial NTO films were grown onto an insulating substrate using a hybrid molecular beam epitaxy technique. The device was patterned using two shadow masks, one for etching with ion milling and the other to deposit metal contacts with sputtering. The ion gel, 1-ethyl-3-methylimidazolium-bis (trifluoromethylsulfonyl) imide (EMI-TFSI), was placed on top of the patterned NTO films and electronic measurements were taken in an electromagnet. Voltage-dependent leakage current through the ionic gel was established, allowing for calculation of injected charge. Temperature-dependent resistivity measurements were performed for each gate bias.

Introduction:
Perovskites, having the general chemical formula of ABO₃, are characterized by a wide range of fascinating functionalities including superconductivity, thermoelectricity and a metal-to-insulator transition. NdTiO₃ (NTO), a pseudo cubic perovskite, is a Mott-Hubbard antiferromagnetic insulator with the insulating state being sensitive to doping and chemical distortions. Past research has found a Mott transition induced by chemical doping using holes [1], although it was accompanied by distortions in the structure. These structural distortions may influence the electronic transport properties of NTO; therefore, this experiment used ionic gel to minimize any distortions in the lattice parameters. This experiment was designed to inject electrons and holes using an external bias to control the insulator to metal transition of NTO.

Experimental Procedure:
A hybrid molecular beam epitaxy technique was used to grow single crystalline, epitaxial neodymium deficient NTO film onto lanthanum aluminate-strontium aluminium tantalite (LSAT), an insulating substrate [2]. A shadow mask was placed over the NTO film and ion milling was used to etch the desired pattern so that Van der Paw geometry could be used to determine resistance. A second shadow mask was positioned to deposit the metal contacts, 40 nm of titanium followed by 100 nm of gold, with sputtering. The ion gel, 1-ethyl-3-methylimidazolium-bis (trifluoromethylsulfonyl) imide (EMI-TFSI), was placed by hand on top of the patterned NTO film, a schematic of the device is shown in Figure 1. The electronic measurements were controlled with a LabView program using a Keithley source-meter K-2400 and electrometer K-6514. Advanced Research Systems cryostat and GMW 5403 electromagnet were used for the temperature dependent measurements. Resistance measurements were taken before device development, once the ion gel was applied and throughout the gating process. The gate voltage was changed at 290 K, when the ion gel was not frozen, and the gate current was measured.
Results and Conclusions:

The gate current was integrated with respect to time to determine the charge injected, verifying that positive gate voltages resulted in electron injection while negative gate voltages resulted in hole injection. The data was not clean due to measuring resistance, thus applying a current too early. This created periodic noise in the data, as seen in Figure 2, which affected the calculation of charge injection.

The resistance data from the experiment was compared to determine the effects of electrostatic gating on NTO. It was determined that positive gate voltages, electron injection, did not change the resistance of the sample, evidenced in Figure 3, while the resistance increased with negative gate voltages, hole injection. At this point it is unclear if these trends are due to electrostatic or electrochemical properties.

NTO thin film was successfully patterned with ion milling and an ion gel was applied. Electrostatic gating resulted in an increase in resistance with hole injection, while electron injection had no observable change in resistance.

Future Work:

In continuing this research, different gate voltages should be examined to develop a better understanding of the entire system. Larger positive gate voltages should be used to determine if NTO can be affected by electron injection using electrostatic gating. Negative gate voltages should be examined in further detail to determine if there is a maximum and at which point it is no longer reversible. The increase in resistance, which accompanied the negative gate voltages, should be examined for evidence of degradation. Other samples of NTO with different neodymium vacancies should be used to determine the effect of stoichiometry. Future research should also examine the effect of ion gel on NTO.

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References:

Optimizing Contact Resistance for Improved MoS$_2$ Device Performance

Justin Goodwill
Physics, Duquesne University

NNIN REU Site: Penn State Nanofabrication Laboratory, The Pennsylvania State University, University Park, PA
NNIN REU Principal Investigator: Dr. Joshua Robinson, Materials Science and Engineering, The Pennsylvania State University
NNIN REU Mentor: Brian Bersch, Materials Science and Engineering, The Pennsylvania State University
Contact: goodwil2@duq.edu, jrobinson@psu.edu, bmb5382@gmail.com

Abstract:
In recent years, much attention has been directed toward two-dimensional materials given their possible applications in next-generation nanoelectronic devices. Graphene, the most widely studied two-dimensional material, has enjoyed major success due to its attractive electronic, thermal, and optical properties. However, graphene lacks a band gap, which renders it unviable for use as a semiconductor in transistor devices. Like graphene, molybdenum disulfide (MoS$_2$) is a two-dimensional material with the exception that it has a tunable 1.2-1.9 eV bandgap. As such, transistor devices have been fabricated using MoS$_2$, but major issues have arisen, including high contact resistance, that have stifled device performance. In this paper, we examine the contact resistances between 7 nm MoS$_2$ films and various metals — including Au, Ti, Ni, Nb, and Mo — using the two-terminal transmission line method. We also investigate the effect of annealing processes on decreasing contact and sheet resistances.

Introduction:

Semiconducting MoS$_2$, one of many transition metal dichalcogenides, exhibits strong intralayer covalent bonding combined with weak interlayer van der Waals bonding. MoS$_2$ has a band gap ranging from approximately 1.9 eV at monolayer thickness to 1.2 eV in bulk, making it ideal for use as a semiconductor in field-effect transistor devices [1]. MoS$_2$ transistors have displayed large current on/off ratios of $10^8$, a subthreshold slope of $60 \text{ mV/dec}$, and a field effect mobility of $10-100 \text{ cm}^2\cdot\text{V}^{-1}\cdot\text{s}^{-1}$ [2].

However, forming true ohmic contacts to MoS$_2$ has proven difficult due to a phenomenon known as Fermi-level pinning. Conventionally for semiconductor-metal interfaces, metals are chosen based on their work function alignment with the semiconductor's conduction band or valence band. In contrast, for the MoS$_2$-metal interface, the Fermi level is partially pinned, resulting in large Schottky barriers for a wide range of metal work functions [2].

Thus, if a metal can be found to not form a large Schottky barrier at the interface, we could significantly enhance device performance.

Experimental Procedure:
Electron-beam evaporation was used to deposit 1-2 nm of Mo on five sapphire substrates. These films were sulfurized in a horizontal tube furnace at 1050°C for 45 minutes. We characterized the films using atomic force microscopy (AFM), Raman spectroscopy, and photoluminescence spectroscopy (PL). AFM indicated a film height of 5-7 nm with 100-200 nm sized grains. A weak PL signal and a Raman peak spacing of ~ 25 wavenumbers also indicated few-layer thick films.

Combined with photolithography, we isolated MoS$_2$ channels by sulfur hexafluoride (SF$_6$) plasma etching of the surrounding film. For our contact study, we deposited five metals with a range of work functions: Au, Ti, Ni, Nb, and Mo. These were chosen based on previous reports of low contact resistance using these metals and based on the fact that some of these metals form similar or identical TMD structures with sulfur (i.e., NbS$_2$ and MoS$_2$) [3-4].

A finished device is pictured in Figure 1. With the photolithography mask, an array of these devices was fabricated such that the channels varied in length from 0.75 µm to 6.5 µm.

The array of devices allowed for two-terminal transmission line measurements (TLM) to be carried out. Using electrical probes, two-terminal current vs. voltage curves were used to calculate the total resistance of all devices. A linear relationship exists between channel length and total resistance such that the y-intercept, corresponding to zero-length channel resistance, allows for the calculation of the contact resistance while the slope allows for the calculation of sheet resistance through the channel. We computed the contact resistance and sheet resistance values using multiple TLM sets for each metal post-deposition, after a 250°C anneal, and after a subsequent...
300°C anneal. All electrical measurements were carried out at room temperature in ambient.

**Results and Conclusions:**

The results for the effect of the annealing processes on Ni are shown in Figure 2. We concluded that the 250°C anneal was an effective heat treatment as for all the metal contacts there were decreases in contact resistance and/or total resistance. While Ti and Mo contacts saw a slight increase in sheet resistance, other metals showed a decrease in sheet resistance to varying degrees. We also observed that the subsequent 300°C anneal was not an effective heat treatment as it either resulted in little change or an increase in all resistance values.

Figure 3 is a table comparing the sheet resistance and contact resistance for each metal. Ti contacts are inconclusive and unreliable due to a significant scatter in the data (low $R^2$) and much smaller sheet resistance than all other samples. The data for Au, Ni, Mo, and Nb contacts display true linear trends. However, negative y-intercept values suggest very low contact resistances.

**Future Work:**

Due to the variation in the data and negative y-intercept values, we plan to repeat TLM measurements in vacuum, after a vacuum anneal, to remove water and other adsorbed species from the MoS$_2$ surface. We will finish gated devices and perform TLM measurements at different gate biases. Gated TLM measurements are crucial for a fair comparison of devices as there is likely to be variation in the doping levels of the films. That is, we will compare the contact and sheet resistances of all devices at the same bias conditions (i.e., at threshold). We will also use smaller channel lengths as they are more accurate for measuring small contact resistances via TLM method.

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**References:**


Enhanced Mobility in an Insulator Capped
2D Electron Gas at SrTiO$_3$ $<$100$>$ Surface

Nathan Huber
Physics, Gustavus Adolphus College

NNIN REU Site: Penn State Nanofabrication Laboratory, The Pennsylvania State University, University Park, PA
NNIN REU Principal Investigator: Prof. Qi Li, Physics, The Pennsylvania State University
NNIN REU Mentors: Dr. Ludi Miao and Renzhong Du, Physics, The Pennsylvania State University
Contact: nhuber2@gustavus.edu, qil1@psu.edu, lxm66@psu.edu, rud145@psu.edu

Abstract and Introduction:
Two-dimensional electron gases (2DEGs) at oxide surfaces and interfaces have attracted much attention due to their fascinating exotic properties such as superconductivity, large magneto-resistance, and ferromagnetism. SrTiO$_3$ (STO) based 2DEGs are a typical example. These include 2DEGs at the interface of LaAlO$_3$/STO heterostructures and on STO surfaces [1]. With their high mobility and high dielectric constant at the ground state, these 2DEGs are promising in developing next generation all-oxide devices including field effect transistors and spintronic devices [2].

In this study we have created 2DEGs at STO $<$100$>$ surfaces by Ar$^+$ ion irradiation. We found that a SiO$_2$ capping layer on the 2DEG surfaces significantly decreased surface resistance, while no effect was observed for other oxide capping layer tests (MgO, Al$_2$O$_3$, and STO). Specifically the electron mobility of the SiO$_2$ capped channel had an eight-fold increase relative to uncapped 2DEG at 1.8 K. The bare channel had a resistance ratio ($R_{300\text{K}}/R_{1.8\text{K}}$) of 85 compared with the SiO$_2$ capped channel ratio of 625; this indicates significantly better metallic behavior for capped channels. Our results open a path to create 2DEGs with high mobility in an effective and economic way.

Experimental Procedure:
2DEG measurement units were fabricated at STO surfaces (Figure 1). First, photolithography was used to pattern a Hall bar. The exposed substrate was then subject to Ar$^+$ ion irradiation (Figure 2). The Ar$^+$ ion irradiation generates oxygen deficiencies at the surface. Carriers were thus increased in order to neutralize charge at the STO surface. Electrical contacts were fabricated by sputtering titanium and gold. The contact patterns were defined by photolithography. Finally the irradiated surface was capped by sputtered SiO$_2$.

Experimental variations were made to the 2DEG. The STO substrate was tested at a SiO$_2$ capped and uncapped state. The dose of ion milling and thickness of capping was also varied. The capping layer effect was tested for several other materials including: MgO, Al$_2$O$_3$, and STO.

The Hall bars allowed for five probe and Hall effect measurements. These measurements were made in a physical property measurement system (PPMS). The sample resistance, carrier density, and mobility were measured as function of temperature from 300 K to 1.8 K.

Figure 1: Standard Hall bar layout used for STO 2DEG fabrication and measurements. A. STO substrate B. Titanium and gold contacts C. Capping layer D. Ion milled STO 2DEG channel.

Figure 2: Ar irradiation (ion milling) reduces STO $<$001$>$ surface to form 2DEG.
Results and Conclusions:

From the resistance measurement, it was found that the capped and uncapped STO 2DEG were fully metallic; this is evident from the decrease in resistance as temperature decreases (Figure 3). It was also observed that the SiO$_2$ capped channel had lower resistance compared to the uncapped channel at all temperatures. The bare channel had a resistance ratio ($R_{300K}/R_{1.8K}$) of 85 compared with the significantly higher SiO$_2$ capped channel’s ratio of 625. This indicates improved mobility in the capped channel.

Several other oxides were tested as capping layers for the possibility of 2DEG enhancement. Among those capping layers tested (MgO, Al$_2$O$_3$, STO, and SiO$_2$), SiO$_2$ was the only material to exhibit enhancement. This observation may be explained with a possible mechanism of band bending at the ion milled STO and SiO$_2$ interface. The shallow work function of SiO$_2$ could potentially bend the conduction band of the STO below the Fermi level. Further theoretical work must be completed to verify this explanation.

It was also observed that terminated STO substrate increased the conductivity in the 2DEG channel. This increase was expected because the terminated substrate has fewer imperfections to hinder electron flow. Observing this increase motivates future research in depositing more uniform coats of SiO$_2$. This could lead to increases in channel conductivity.

Finally it was observed that decreasing the ion milling duration and capping layer thickness led to decreases in carrier density of the 2DEG. This is important information because control of conductive channels with low carrier density would be applicable for future field effect transistors.

These results introduce SiO$_2$ capping of STO 2DEG as a promising method for fabrication of oxide conductors. The enhancement of mobility obtained by this capping has significant implications for oxide electronics.

Future Work:

In the future, the Li research group will continue the characterization of SiO$_2$ capped STO 2DEG. To attain increased mobility, the group plans to explore SiO$_2$ capping thickness and uniformity. Basic control of carrier density has been observed by way of gating techniques. Further increasing the mobility and control of the carrier density in this 2DEG would be important for future applications.

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References:


Fiber Flow Rate Sensors Using Thermally Drawn Multi-Material Fluidic Channel Fibers

Corey Kwok
Materials Science Engineering, Purdue University

NNIN REU Site: Microelectronics Research Center, The University of Texas, Austin, TX
NNIN REU Principal Investigator: Dr. Zheng Wang, Electrical and Computer Engineering, University of Texas at Austin, TX
NNIN REU Mentor: Boxue Chen, Electrical and Computer Engineering, University of Texas at Austin, TX
Contact: corey.g.kwok@gmail.com, zheng.wang@utexas.edu, boxuechen@gmail.com

Abstract:
Thermally drawn multi-material fibers with conductive polyethylene (CPE) film incorporated fluidic channels were developed. The initial resistivity of CPE was recorded as 0.35 Ω m and 0.18 Ω m after fiber draw. The effect of flow rate on their resistance was observed. The “in fiber” flow sensor can determine the flow rate with a sensitivity of 5.237*10^5 µV/µL·min⁻¹ in the 0-40 µL/min range at bias current 1 mA.

Introduction:
Preforms made up of polycarbonate (PC) slabs and conductive polymer films are drawn into fibers by heating the mold while pulling the preform through the furnace. This method maintains the preform's cross sectional geometry proportionally based on a set reduction ratio (16 to 17 times smaller) [1]. Conductive polyethylene (CPE) film contains carbon black mixed with the polyethylene chain structure. Carbon black is made up of highly conductive fine carbon particles. These particles form conductive pathways in between polymer chains [2]. As water flow cools a resistor, the measured resistance will be less than initially. This change is characterized for a range of flow rates and the flow sensor uses the relation to determine the flow [3]. By containing the process within the fiber, the sensor can be integrated into various applications such as lab equipment, catheters, and fuel injectors [4].

Experimental Procedure:
CPE film was cut to five different lengths, 1-6 cm long and 1.27 cm wide. Resistance was recorded using a four point probe method with four silver paint contact points on each sample [5]. A power supply generated a 0.01 mA current and the voltage across the inner contact points was recorded. The relation between resistance and length denotes the resistivity of CPE film.

Two PC slabs 38.1 mm wide, 381 mm long, and 5.35 mm thick were place on top of another and then wrapped twice with CPE film. The preform is thermally drawn down to a 2 mm wide fiber. CPE is removed so that only one surface is covered to ensure the dimensions of the film. The resistivity of CPE, as a fiber, is determined using the four point probe method with five different lengths at the same current of 0.01 mA.

Two PC slabs individually wrapped three times with CPE film with smaller slabs are placed in between leaving a gap between them. The preform is thermally drawn and reduced to a 1 mm fluidic channel in a 2 mm wide fiber. CPE is removed such that only the resistance of the inner channel layers are measured. Plastic tubing added to both ends to prevent shorting equipment.

A syringe pump induced 0-1000 µL/min of water flow into the channel fiber samples. Flow rate is generated based on the total volume and length of the syringe. Along with the four point probe power supply setup, the resistance was measured at incrementing flow rates.

Results and Conclusions:
The resistivity of CPE decreased from 0.35 to 0.18 Ωm after thermal drawing. Similar sample sets have a consistent resistivity. The thickness and width of the CPE layers in the fiber samples varied greatly. In Figure 2, at lengths beyond 1.5 cm, the conductive pathways become more complex and less linear resulting in a wider range of resistance. In Figure 3, an exponential relation between flow rate and resistance results from the convective cooling process that cools exponentially with flow rate.

This CPE channel design should be only applied in the 0-40 µL/min range because this range produces the most linear data. Within this range we can more precisely determine the flow rate with a sensitivity of, 5.237*10^5 µV/µL/min, higher than other micro sensors.
The channel fiber has comparable range but greater power consumption (76 mW) due to high current for increasing the initial resistance [6].

**Future Work:**
An automated setup for determining the response time. Verify the consistency of our results by testing fiber draws using the same preform design to explore the possibility customizing the resistivity of fibers. Vary the amount of layering of CPE or PC film insulation in the channel fiber to lessen the cooling rate and increase the resistance for a larger flow rate range. A proof of concept to demonstrate the easy integration the in fiber design professes.

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**References:**
Optimizing Insulator Layer Deposition for Diamond MOSFETs

Tara Nietzold  
Materials Science and Engineering, Rutgers University

*NNIN iREU Site: National Institute for Materials Science (NIMS), Tsukuba, Ibaraki, Japan*  
NNIN iREU Principal Investigator: Yasuo Koide, Center of Materials Research for Low Carbon Emission, NIMS  
NNIN iREU Mentor: Masataka Imura, NIMS, Tsukuba, Ibaraki, Japan  
Contact: ttmn313@aim.com, koide.yasuo@nims.go.jp, imura.masataka@nims.go.jp

**Abstract:**

Field effect transistors (FETs) are important components in electronic devices due to their ability to act as electrical switches. They are comprised of a source, drain and gate, and there must be enough energy potential difference in order for the carriers, electrons or holes, to flow from the source to the drain. One of the ways the effectiveness of these devices can be improved is by applying an insulator or oxide layer on top of the channel layer in order to reduce the number of carriers that escape through the gate contact. In the case of this research, aluminum oxide was analyzed for its application as an oxide layer in these devices.

![Figure 1: A graphic depicting the cross-sectional structure of the fabricated MOS devices.](image1)

**Introduction:**

It has been found that diamond can be used as a viable substrate for fabricating both field effect transistor devices and diode devices. This is because it is a wide band gap material with a high degree of hardness, thus making it ideal in high-power applications. Additionally, diamond has the ability to have a hydrogen-terminated surface providing it with a high concentration of holes that then act as the carriers in the device. So in a metal oxide semiconductor field effect transistor, or MOSFET, the diamond behaves as the base semiconductor.

![Figure 2: A microscope image of a fabricated FET (left) and diode (right). It should be clear to see the individual source, gate, and drain pairs for the individual FET devices.](image2)

Figure 1 shows the current device set up, including demarcations for the source (S), the drain (D), the gate (G), and the gate oxide, aluminum oxide (Al₂O₃). In the image, it also shows two diamond layers, the bulk layer and an epilayer. This epilayer is a high-quality layer that improves the quality of the contacts that are made.

**Procedure:**

The fabrication process was a multi-step process beginning with the development of the H-terminated surface, which was done through microwave plasma chemical vapour deposition. This also created the diamond epilayer on the bulk diamond to improve the surface quality. Afterwards, photolithography, followed by dry etching and electron gun evaporation, was used to deposit the metals for the key pattern, the mesa structure for the fabricated FETs, and the source and drain. The metals used were titanium, platinum, and then gold.

After the source and drain were completed, the oxide layer of Al₂O₃ was deposited by means of atomic layer deposition (ALD). Three different deposition temperatures were used in order to understand the influence of temperature on the deposition quality and furthermore, on the total current output. After the ALD, photolithography and e-gun...
evaporation were used again in order to create the metal component of the gate. Finally, the samples were annealed in order to improve the drain current values.

A set of successfully fabricated MOSFETs and MOS diodes can be seen in Figure 2.

Results and Conclusion:
The electrical properties of the Al$_2$O$_3$/H-diamond based metal-oxide-semiconductor (MOS) diodes and MOSFETs were studied. This was done by using a semiconductor probe measuring system where contacts were made to the source, drain and gate, and then the total current observed in the drain was measured. Based on the results, it was found that there exists an ideal deposition temperature range for the Al$_2$O$_3$.

The best results were found when the oxide was deposited at 300°C, because it produced ideal capacitance-voltage behavior without flat-band shift in the MOS-diode devices. Figure 3 shows the shift in the hysteresis curve as the deposition temperature was varied.

Additionally, the MOSFET showed good operation with normally-on, ohmic characteristics. The standard drain current versus voltage (IV) was expected to have a linear piece beginning at the origin, before it plateaued into the saturated region. Figure 4 shows an IV-curve for an FET device fabricated at 300°C and then annealed for an hour at 180°C. The maximum drain current it produced was -7.0 mA/mm, which is relatively low.

Future Work:
After establishing a reliable deposition technique and discovering the existence of the ALD temperature window, the next steps are to continue to manipulate the ALD parameters and observe the maximum drain current that is produced. Once devices with a reasonable drain current can be produced and reproduced, it will be able to prove diamond to be a practical and beneficial MOSFET semiconductor substrate.

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References:

Figure 3: An overlay of the capacitance dependence found for devices fabricated at 120°C, 300°C, and 390°C. The shift in the curve represents an existence of positive charges (shifted left) and negative charges (shifted right), which are not desired.

Figure 4: A drain current versus voltage curve for the 300°C trial.
Graphene Junction Field-Effect Transistors on a Silicon Carbide Substrate

Andrea Randolph
Chemical and Biological Engineering, University of Colorado Boulder

NNIN REU Site: Colorado Nanofabrication Laboratory, University of Colorado, Boulder, CO
NNIN REU Principal Investigator: Dr. Bart Van Zeghbroeck, Electrical and Computer Engineering, University of Colorado Boulder
NNIN REU Mentor: Tzu-Min Ou, Electrical and Computer Engineering, University of Colorado Boulder
Contact: andrea.randolph@colorado.edu, bart@colorado.edu, tzumin.ou@colorado.edu

Abstract:
Quantum mechanics predicts that the advancement of silicon transistors will soon reach its physical limit and thus a replacement transistor material is needed. We investigated silicon carbide (SiC) for this use due to its compatibility with existing semiconductor fabrication methods and with graphene growth processes. Graphene was chosen as a channel material due to its superior charge carrier properties. It can be either epitaxially grown directly on the SiC substrate or grown on metal and then transferred. We explored the viability of both types of graphene as laterally-conducting channels for junction field effect transistors (JFETs) on SiC substrates. The direct contact between our channel and semiconductor created a unique and novel heterojunction. The epitaxial graphene JFETs (epi-GJFETs) failed to modulate current due to discontinuity between the electrodes; however, our transferred-graphene JFET (GFET) devices were functional. An additional degree of freedom for current control was created compared to traditional transistors since the channel conductivity can be tuned by altering the applied voltage and the Dirac voltage can be tuned by altering the substrate doping. Our JFET design is compatible with other two-dimensional materials.

Introduction:
Transistors are extensively used in mainstream electronics and are primarily fabricated on silicon substrates. Until now, we have been able to produce increasingly smaller transistors; however, a quantum effect referred to as “charge tunneling” will soon limit this continual smaller scaling [1]. As a widely-researched hexagonal allotrope of carbon, graphene (G) has potential for use as a semiconductor channel material due to its superior charge carrier properties, including over 100× greater mobility and 30× faster velocity than silicon [2]. As a two-dimensional material, graphene carries current laterally and avoids vertical charge dissipation [3]. Graphene tends to be chemically p-doped by air, so we chose heavily n-doped SiC for our underlying substrate.

As seen in Figure 1, our GJFETs consisted of a graphene channel lying across the SiC substrate, atop which the source and drain electrodes rested. We chose to design JFETs over the more widely-used metal-oxide-semiconductor field effect transistors (MOSFETs) because our devices were back-gated and lacked oxide insulation layers.

These JFET devices are always on and require an applied voltage at the gate to turn the device off: moving electrons from the n-doped SiC into the holes of the p-doped graphene induces a depletion region where no carriers are present, eventually growing large enough to decrease the conductivity and cut off the charge flow.

Fabrication Procedure:
The fabrication procedure for our epitaxial GJFETs is shown in Figure 2 (a) and for our transferred GJFETs in (b). Our epi-G on SiC samples were commercially prepared by thermal decomposition.

We patterned and etched channels into the top graphene layer using optical lithography followed by oxygen plasma, respectively. We then blanket evaporated nickel on the backside to create the gate. Photoresist insulating layers
were added, and then finally the chrome/gold (Cr/Au) source and drain electrodes were deposited by thermal evaporation. The transferred GJFET process was similar, but first involved growth of a graphene layer on a copper (Cu) substrate and then a transfer process. This was done using a polymethylmethacrylate (PMMA) layer and electrolysis to separate the graphene sheet. The SiC wafer was oxidized and back-gated with nickel (Ni) by thermal evaporation. The graphene was then applied to our SiC wafer and annealed so it would fold into the oxide template channels. Finally, we removed the excess graphene, added the top Cr/Au electrodes, and began our probe tests.

**Results and Conclusions:**

The epi-GJFET failed to modulate current. The IV curve in Figure 3 shows that all the applied gate voltage leaked out the drain, without traveling through the graphene channel to the source as desired. We would need some of this voltage to travel through from source to drain in order to induce the depletion region, decrease conductivity, and shut the device off.

From the AFM phase scan, it appears that the graphene channel was non-continuous and that bare SiC was exposed in between the source and drain electrodes. We suspect that either the fabrication process or contamination may have removed the graphene there, resulting in non-functional devices.

In contrast, the transferred GJFET did demonstrate the expected behavior (Figure 4 (a)). The parabolic shape of this curve is indicative of graphene’s progression from p-doped through the turn off Dirac voltage, and then to n-doped. We achieved microamp current in our channel, and an on/off ratio of approximately 2. Our results (Figure 4 (b)) were obtained using SiC with a doping density of about 10^{16} cm^{-3}; previous work done by my mentor using a SiC wafer with a doping density of 10^{19} cm^{-3} shows similar behavior (Figure 4 (c) and (d)).

We successfully introduced a second degree of freedom for tuning channel conductivity: not only can we vary the applied voltage, but we can also additionally change the doping density for further modulation. Our best finished device demonstrated a sheet resistance of 3.33 kΩ/sq, a hole mobility of 2000 cm²/(V·s), and an initial hole density of 1.5 × 10^{12} cm^{-2}. We were unable to extrapolate far enough to obtain the electron mobility.

Our devices show the feasibility of modulating current using GJFETs on a SiC substrate.

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**References:**


Evaluation of TiO$_2$ as Carrier Selective Contact for High Efficiency Photovoltaic Applications

Alexander Rosner
Electrical Engineering, University of Notre Dame

**NNIN REU Site:** ASU NanoFab, Arizona State University, Tempe, AZ

**NNIN REU Principal Investigator:** Dr. Mariana Bertoni, Electrical Engineering, Arizona State University

**NNIN REU Mentor:** Dr. Laura Ding, Electrical Engineering, Arizona State University

**Contact:** arosner@nd.edu, mariana.bertoni@asu.edu, laura.ding@asu.edu

**Abstract:**
Herein we evaluate titanium dioxide (TiO$_2$) as a carrier selective contact for silicon solar cells. Additionally, we investigate aluminum oxide (Al$_2$O$_3$) as a dedicated passivation layer that could be combined with TiO$_2$ for improved performance. Using a photoconduction lifetime tester, we found that TiO$_2$ presents a poor passivation of the silicon surface and that the best minority carrier lifetime was achieved on an 8 nm thick Al$_2$O$_3$ layer annealed in forming gas. We then created heterojunction with intrinsic thin (HIT) solar cells using TiO$_2$ as the electron carrier-selective contact, and found low open-circuit voltages and efficiency consistent with the poor surface passivation.

**Introduction:**
The most efficient silicon solar cell today uses amorphous silicon (a-Si) to passivate the surface and selectively collect carriers from the c-Si. However, a-Si absorbs some of the light that the c-Si could turn into carriers. We investigated TiO$_2$ as a replacement candidate since, with a band gap of 3.2 eV, it is transparent to visible light and its bandstructure theoretically should line up with c-Si’s, making it a good electron-selective contact [1]. However, TiO$_2$’s ability to prevent surface recombination of minority carriers is variable and our project’s aim was to quantify it.

**Experimental Procedure:**
We prepared TiO$_2$ and Al$_2$O$_3$ films using thermal atomic layer deposition (ALD) on n-type Czochralski c-Si wafers after removing the native oxide. We varied the deposition temperature and film thickness to investigate the relationship between films’ properties and passivation capability. Next, we annealed the wafers to activate the passivation and varied the annealing temperature, duration and atmosphere (air or forming gas). The films were deposited on both sides of the wafer for lifetime measurement, while only on the back side of the cells.

We evaluated surface passivation of c-Si by quasi-steady-state photoconductance decay measurements to extract the minority carrier lifetime, at a minority carrier density (MCD) of $1 \times 10^{15}$ cm$^{-3}$.

We report effective lifetimes ($\tau_{eff}$), which account for bulk and surface lifetimes. Solar cell performances were characterized by current-voltage and by external quantum efficiency (EQE) measurements.

**Results and Conclusions:**
The effective lifetimes of the different thicknesses of TiO$_2$ prepared at different temperatures are presented in Figure 1, for the as-deposited state and after annealing. The highest lifetimes originate from the thinnest coatings, and annealing has only a minor effect for 3 min, while a drop in lifetime was observed for 30 min. The detrimental impact of thicker layers and longer annealing is possibly related to stress-induced phase transformation leading to more defects in the films and a higher recombination rate [2]. The deposition temperature seems to have no effect on the passivation quality. Using TiO$_2$, we could only achieve a surface recombination velocity of 70 cm.s$^{-1}$, whereas a-Si can produce > 1 cm.s$^{-1}$ (15 cm.s$^{-1}$ in our case).

We prepared cells with the best TiO$_2$ films—8 nm (230°C), 5 nm (180°C), 6 nm (130°C)—as the electron-selective contact. Figure 2 shows the EQE of the best cell compared to two reference cells, a standard HIT and HIT with Al back. At higher wavelengths, the current generated by the cell with TiO$_2$ is lower than that of the references mainly because of a difference in back side light reflection.

Figure 3 shows a table of the solar cells’ performance. The TiO$_2$ thickness-dependence was only observed in the fill factor (FF), due to the high resistivity of TiO$_2$ (typically $\sim 10^5$ Ω.cm), with the thinnest TiO$_2$ layer resulting in a FF as high as the reference cells. All open-circuit voltage ($V_{oc}$), short circuit current density ($J_{sc}$) and efficiencies were lower than for the reference cells. The $V_{oc}$ of the best TiO$_2$ cell was 564 mV, which is comparable to the implied $V_{oc}$ value (given by the lifetime tester as the highest $V_{oc}$ attainable by the cell if passivation is the only limiting
factor) of 580 mV. This demonstrates that the passivation and not the carrier selectivity is the most significant factor in poor cell performance. Therefore, Al$_2$O$_3$ was investigated as an alternative passivation coating.

In Figure 4, we show the lifetime of Si wafers with different thicknesses of ALD Al$_2$O$_3$ against different annealing conditions. We found that 8 nm thick films lead to the best lifetime > 1 ms after a 15 min 425°C anneal in forming gas. Although annealing in air revealed that thicker layers (15 and 3 nm) result in better passivation as they contain more hydrogen to passivate the dangling silicon bonds, this advantage decreases when hydrogen can be provided by annealing in forming gas [3]. Moreover, thicker layers may suffer from increased stress, explaining why the 8 nm thick film gave the best passivation.

In summary, we found that the poor passivation ability of TiO$_2$ on silicon for a wide range of depositions and post-deposition treatment conditions resulted in underperforming solar cells, however the passivation ability of Al$_2$O$_3$ seems to be comparable to α-Si, presenting a potential path for high efficiency devices.

**Future Work:**
We would like to combine Al$_2$O$_3$ and TiO$_2$ layers, and implement them at the sun-facing side instead of backside to improve passivation and benefit from higher transparency than the α-Si layers. Changing the deposition method or trying different post-deposition treatments such as light-soaking could improve the passivation ability of TiO$_2$.

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**References:**