

Graphene Junction Field-Effect Transistors on a Silicon Carbide Substrate

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Abstract:

Quantum mechanics predicts that the advancement of silicon transistors will soon reach its physical limit and thus a replacement transistor material is needed. We investigated silicon carbide (SiC) for this use due to its compatibility with existing semiconductor fabrication methods and with graphene growth processes. Graphene was chosen as a channel material due to its superior charge carrier properties. It can be either epitaxially grown directly on the SiC substrate or grown on metal and then transferred. We explored the viability of both types of graphene as laterally-conducting channels for junction field effect transistors (JFETs) on SiC substrates. The direct contact between our channel and semiconductor created a unique and novel heterojunction. The epitaxial graphene JFETs (epi-GJFETs) failed to modulate current due to discontinuity between the electrodes; however, our transferred-graphene JFET (GFET) devices were functional. An additional degree of freedom for current control was created compared to traditional transistors since the channel conductivity can be tuned by altering the applied voltage and the Dirac voltage can be tuned by altering the substrate doping. Our JFET design is compatible with other two-dimensional materials.

Introduction:

Transistors are extensively used in mainstream electronics and are primarily fabricated on silicon substrates. Until now, we have been able to produce increasingly smaller transistors; however, a quantum effect referred to as “charge tunneling” will soon limit this continual smaller scaling [1]. As a widely-researched hexagonal allotrope of carbon, graphene (G) has potential for use as a semiconductor channel material due to its superior charge carrier properties, including over 100× greater mobility and 30× faster velocity than silicon [2]. As a two-dimensional material, graphene carries current laterally and avoids vertical charge dissipation [3]. Graphene tends to be chemically p-doped by air, so we chose heavily n-doped SiC for our underlying substrate.

As seen in Figure 1, our GJFETs consisted of a graphene channel lying across the SiC substrate, atop which the source and drain electrodes rested. We chose to design JFETs over the more widely-used metal-oxide-semiconductor field effect transistors (MOSFETs) because our devices were back-gated and lacked oxide insulation layers.

These JFET devices are always on and require an applied voltage at the gate to turn the device off: moving electrons from the n-doped SiC into the holes of the p-doped graphene induces a depletion region where no carriers are present, eventually growing large enough to decrease the conductivity and cut off the charge flow.

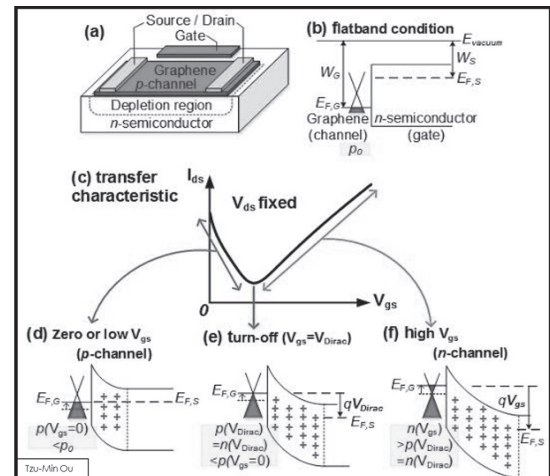


Figure 1: (a) GJFET schematic, (b) energy band diagram for the graphene-semiconductor heterojunction, (c) transfer characteristic curve showing graphene's transition, (d) from an initially on p-doped device, (e) to the neutral turn-off condition, and (f) to an n-doped channel.

Fabrication Procedure:

The fabrication procedure for our epitaxial GJFETs is shown in Figure 2 (a) and for our transferred GJFETs in (b). Our epi-G on SiC samples were commercially prepared by thermal decomposition.

We patterned and etched channels into the top graphene layer using optical lithography followed by oxygen plasma, respectively. We then blanket evaporated nickel on the backside to create the gate. Photoresist insulating layers

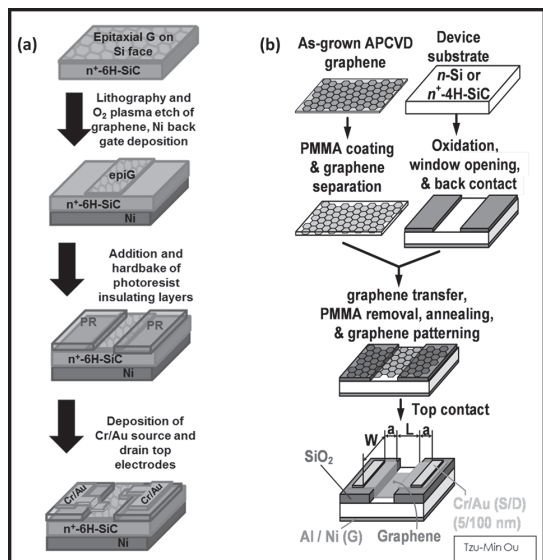


Figure 2: Fabrication steps for (a) an epi-GJFET and (b) a transferred G-JFET.

were added, and then finally the chrome/gold (Cr/Au) source and drain electrodes were deposited by thermal evaporation. The transferred GJFET process was similar, but first involved growth of a graphene layer on a copper (Cu) substrate and then a transfer process. This was done using a polymethylmethacrylate (PMMA) layer and electrolysis to separate the graphene sheet. The SiC wafer was oxidized and back-gated with nickel (Ni) by thermal evaporation. The graphene was then applied to our SiC wafer and annealed so it would fold into the oxide template channels. Finally, we removed the excess graphene, added the top Cr/Au electrodes, and began our probe tests.

Results and Conclusions:

The epi-GJFET failed to modulate current. The IV curve in Figure 3 shows that all the applied gate voltage leaked out the drain, without traveling through the graphene channel as desired. We would need some of this voltage to travel through from source to drain in order to induce the depletion region, decrease conductivity, and shut the device off.

From the AFM phase scan, it appears that the graphene channel was non-continuous and that bare SiC was exposed in between the source and drain electrodes. We suspect that either the fabrication process or contamination may have removed the graphene there, resulting in non-functional devices.

In contrast, the transferred GJFET did demonstrate the expected behavior (Figure 4 (a)). The parabolic shape of this curve is indicative of graphene's progression from p-doped through the turn off Dirac voltage, and then to n-doped. We achieved microamp current in our channel, and an on/off ratio of approximately 2. Our results (Figure 4 (b)) were obtained using SiC with a doping density of about 10^{16} cm^{-3} ; previous work done by my mentor using a SiC wafer with a doping density of 10^{19} cm^{-3} shows similar behavior (Figure 4 (c) and (d)).

We successfully introduced a second degree of freedom for tuning channel conductivity: not only can we vary the applied voltage, but we can also additionally change the doping density for further modulation. Our best finished device demonstrated a sheet resistance of $3.33 \text{ k}\Omega/\text{sq}$, a hole mobility of $2000 \text{ cm}^2/(\text{V}\cdot\text{s})$, and an initial hole density of $1.5 \times 10^{12} \text{ cm}^{-2}$. We were unable to extrapolate far enough to obtain the electron mobility.

Our devices show the feasibility of modulating current using GJFETs on a SiC substrate.

Acknowledgments:

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References:

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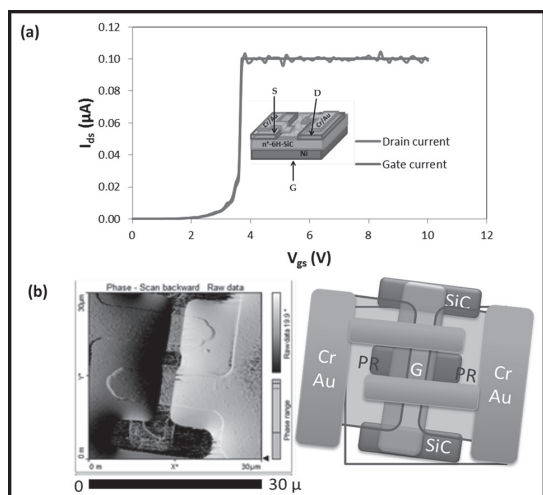


Figure 3: Epi- GJFET (a) transfer curve and (b) AFM phase image of the devices and reference.

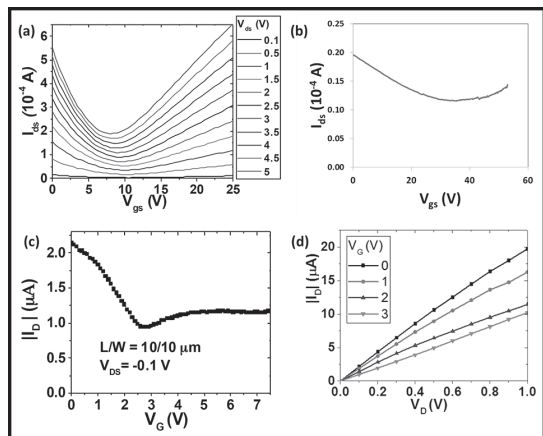


Figure 4: (a) Simulated transfer curve for Si, (b) actual SiC transfer curve ($N_d=10^{16}$), (c) Tzu-Min Ou's transfer curve ($N_d=10^{19}$), (d) Tzu-Min Ou's output curve ($N_d=10^{19}$).