Electrical, Optical, and Thermofluidic Wafer-Level Chip I/O Interconnects Enabled by Nano/Microimprint Lithography

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Abstract:

The increasing demands of silicon microprocessor technology on current delivery (>400A), chip input/output (I/O) bandwidth (>50 Tb/s), and heat removal (200W/cm^2), have affected a need for the development of compatible electrical, optical and thermofluidic chip I/O interconnections (or multimodal I/O).

The goal of this project is to develop low cost wafer-level batch fabrication techniques for multimodal I/O interconnections using nano/microimprint lithography technology. The fabrication of these structures involves spin coating and soft baking a thick, photodefinable polymer film, subsequently transforming the surface topology of the film using nano/microimprinting, and finally UV irradiation through a pattered mask, followed by hard baking and spray developing. General fabrication techniques for nano/microimprinting have been developed, both in template fabrication, with features as deep as 25μm, and in demolding, for which various anti-adhesion layers have been tested. We have successfully produced the following unique interconnect structures: (1) surface-normal optical waveguides terminating in mirrored tips to be used as dual-mode pins, transmitting electrical and optical signals simultaneously, (2) board level, funnel-shaped sockets to hold and align dual-mode polymer pins, and (3) thermofluidic back-side heat sinks compatible with dual-mode pins. The development of these processes has also introduced the possibility of using nano/microimprint lithography in further applications.

Introduction:

As silicon microprocessor technology continues to advance according to Moore's Law, the performance of these high performance chips become limited by interconnects performing communication functions. There are three system level limiting interconnect technologies to chip performance: (1) current deliver (>400A), heat removal (>100W/cm^2), and chip input/output (I/O) bandwidth (>50Tb/s). These factors have incited a need for the development of electrical, optical, and thermofluidic chip I/O interconnects to enable each of the above listed challenges, respectively.

The goal of the project is to develop wafer-level batch fabricated electrical and optical chip I/O interconnections and methods of attaching these to the board. The strategy for achieving this was the fabrication of an array of slant tip pillars which will function as both electrical and optical means of signal transmission between chips, described as a Sea of Polymer Pillars (SoPP) in previous research [1]. These pillars will be held in place on the printed wiring board by board-level funnel shaped sockets. A schematic of this can be seen in Figure 1. Imprinting would be ideal for this process as it would allow the batch fabrication of these interconnect structures, allowing for patterning submicron features using easy processing [2] as a low cost, high throughput alternative to lithography [3].

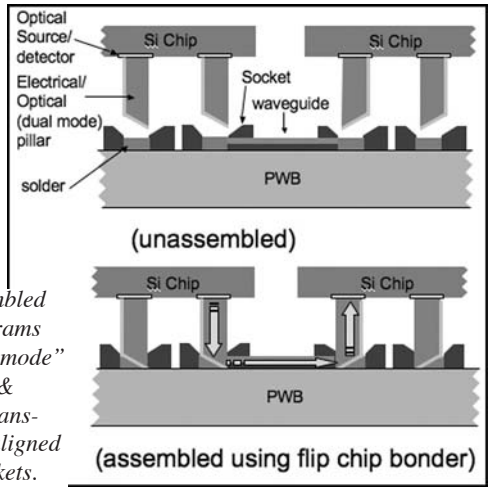

Figure 1: Unassembled & assembled diagrams for slant tip "dual mode" pillars for optical & electrical signal transmission held and aligned by board level sockets.

Fabrication:

A. Template Fabrication:

The first set of fabrication processes created templates to be used during imprinting. This was done by spinning positive resist on a SiO_2 coated silicon wafer, soft baking at 100°C for 2 minutes, then patterning using a mask. The wafer was then developed, and the SiO_2 was etched using BOE, and the silicon was subsequently etched using TMAH. The sample to be imprinted was prepared by spinning a layer of Avatrel 2000P polymer onto a SiO_2 or SiN coated substrate, at varying thicknesses depending on the desired height of the structure, then soft baked at 100°C, then at 125°C. Following the fabrication, the template is coated with a layer of trifluropropyldimethylchlorosilane (TFS), a low surface tension coating for anti-adhesion purposes.

B. Imprinting Process and Interconnect Fabrication:

A nanoimprint tool manufactured by Obducat was used to compress, and subsequently demold, the template from the

polymer coated substrate. Upon separation, the surface of the polymer is imprinted with the inverse template pattern.

Pillars were fabricated by imprinting a 100 μm thick polymer with a channel template, UV exposing the imprinted polymer through a mask, and finally developing and curing to create an array of pillars with patterned tips. The pillars were then metal coated. To fabricate the sockets with which to hold these pillars, a 12 μm layer of polymer was imprinted with a template consisting of an array of 5 μm tall cylindrical structures. The sample was then aligned and UV exposed through a mask, and developed and cured.

During the course of this project, it was discovered that fluidic channels would be fabricated using similar methods, and could be integrated directly on the backside of the chip. To make these channels, a thick polymer layer was spun and imprinted using a channel template. The imprinted sample was then metal coated, then soldered to a blank silicon wafer to create polymer based microfluidic channels.

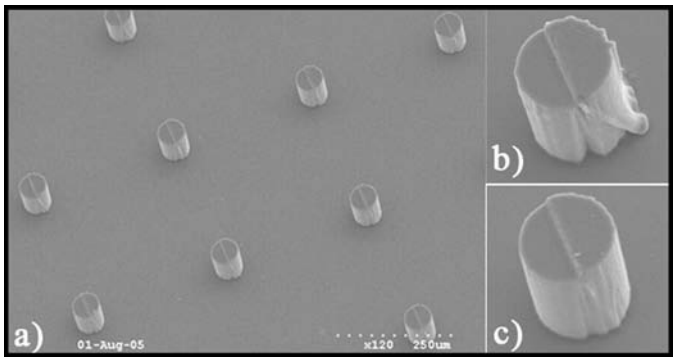

Figure 2: a) Array of slant tip pillars; b) Pillar with un-even UV exposure; c) Pillar UV exposed evenly by immersing in water.

Results and Conclusions:

Arrays of 80 μm tall pillars were fabricated successfully, as seen in Figure 2a. One problem encountered during fabrication was the uneven UV exposure due to the imprinted slant, which provided a surface for refraction of light, and resulted in exposure of polymer beyond the area of the pillar. Because the imprinted slant was at an angle of 54.7°, according to Snell's Law, $n_1 \sin\Theta_1 = n_2 \sin\Theta_2$, incoming UV light would be refracted at an angle of 33.0° from the normal. The result was pillars with extra polymer "tails" (Figure 2b). This issue was successfully resolved by immersing the imprinted polymer surface in water during UV exposure, to provide a surface with a uniform index of refraction (Figure 2c).

Optical transmission measurements were then made on a metallized pillar array constructed on a glass substrate by illuminating the backside of the substrate and recording images using a CCD camera. As seen in Figure 3, the optical transmission in the area of the slant was very low, indicating the ability to use these pillars for optical purposes.

Sockets were fabricated (Figure 4), with a funnel-like shape created by imprinting. These sockets will greatly simplify pillar-to-board mechanical alignment, and are designed to self correct for any misalignment, solving what

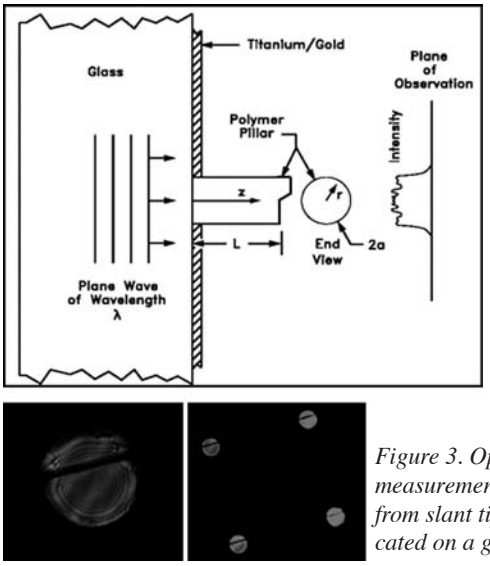

Figure 3. Optical transmission measurement setup & results from slant tip pillars fabricated on a glass substrate.

the ITRS 2005 calls a key issue in assembly. Preliminary results were achieved for the polymer based microfluidic channels. The development of these processes has had a broad impact by introducing the possibility of using nano/microimprint lithography in a number of applications. For example, the unique fabrication process described above was used to fabricate waveguides terminated with mirrors in another REU project [4].

In summary, this is the first demonstration of wafer-level batch fabrication of electrical, optical and thermofluidic I/O interconnects. The fabrication of the three structures listed above will help to address issues of power delivery, heat removal, as well as high chip input/output bandwidth. Future work should include characterization and measurements of these structures.

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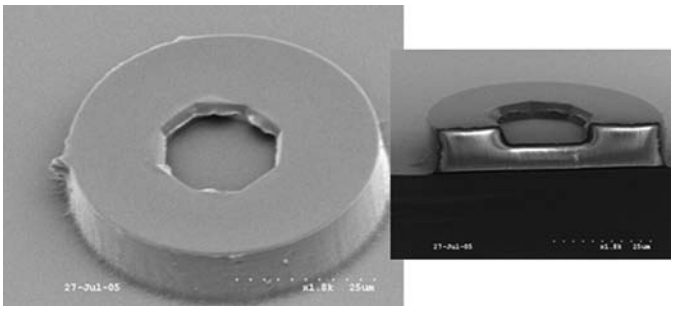

Figure 4. Funnel shaped socket structure and cross section (inset) with inner slope formed by imprinting.