Nonvolatile Memory with Multi-Stack Nanocrystals as Floating Gates

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Abstract

Nonvolatile memory technologies are focusing on devices with longer retention, faster read and write, higher bit density, improved endurance, and low-voltage program/erase characteristics. Nanocrystal (NC) memories are promising for realizing high-density nonvolatile storage with the inherent advantage of low-voltage operation [1]. Recently carbon molecules in the form of fullerenes (C_{60}), known as "bucky balls," also have been incorporated in non-volatile memory devices [2] with its advantages of mono-disperse nature and molecular size. In this project, various memory structures with self-assembled multi-stacked gold, platinum, and C_{60} nanocrystals as floating gates have been fabricated and characterized. In two-layer nanocrystal structures, the C_{60} bottom layer acts as an additional barrier to prevent charge back-tunneling from the upper layer, improving retention time without a commensurate penalty in program time. The upper nanocrystal layer functions as additional charge storage to provide sufficient memory window.

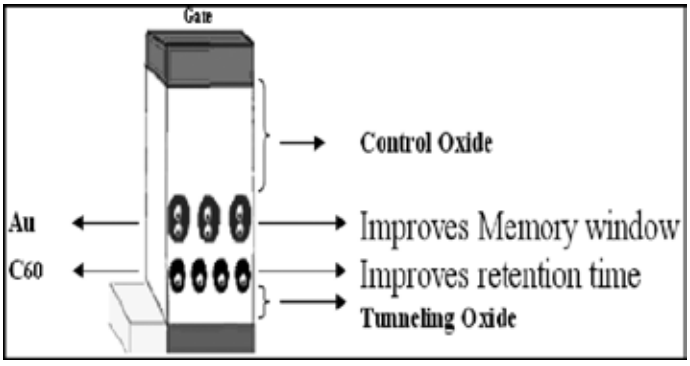

Figure 1: Schematic of the double-layer nanocrystal memory.

Introduction

Figure 1 shows the cross section of a double-layer nanocrystal memory device. By applying enough positive bias across the gate, electrons will quantum-mechanically tunnel through the thin tunneling oxide. If the lower-layer nanocrystal is designed so that it is energetically unfavorable for charge storage due to its small size, electrons will step through the lower nanocrystal layer, and get stored in the second layer nanocrystal. After taking away the applied potential, the energy penalty for electrons in the second layer to tunnel back into the first layer is larger enough, again due to the large charging energy associated with the small size. The first-layer nanocrystal acts as a part of tunneling barrier to provide prolonged retention time. The same concept applies to the hole storage when negative bias is applied. Charging nanocrystals with electrons and holes can require different gate biasing due to different properties of nanocrystals, which also contribute to different retention time characteristics.

The goal was to engineer the best structure such that one can obtain a memory device with an optimal memory window and retention time. This required the optimization of the tunneling oxide thickness, nanocrystal diameter and the choice of a nanocrystal material.

Experimental Procedure

P-type wafers with a doping level of 10^{15} cm^{-3} were used in this study. The device isolation was achieved by the local oxidation isolation (LOCOS). 2-3 nanometers of tunneling oxide was grown on the active region in a diluted oxygen ambience using an atmospheric-pressure furnace. Each wafer was named separately.

Sample 1 (S_1) was the control device without any floating gate, sample 2 (S_2) had a single-layer gold (Au) nanocrystal as a floating gate, S_3 had a double-layer Au nanocrystal floating gate, S_4 had a single-layer C_{60} nanocrystal floating gate, S_5 had a double-layer C_{60} and Au nanocrystal floating gate, and S_6 had the same structure as S_5 but with a thinner thickness of tunneling oxide.

The Au nanocrystals were deposited through e-gun evaporation while the C_{60} nanocrystals through the thermal evaporation. For those samples with double-layer nanocrystals, 2-3 nm of evaporated silicon dioxide (SiO_2) was inserted between two layers. After the floating-gate formation, 20-30 nm of control oxide was deposited through a plasma-enhanced chemical vapor deposition (PECVD), followed by chromium and aluminum evaporation as the control gate. Finally the control gate was patterned to finish the device fabrication. The device was now measured, and memory window and retention time for different configurations were compared.

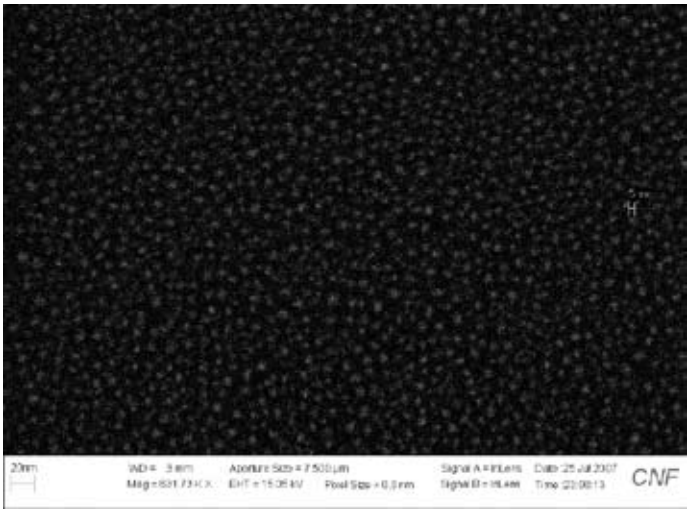

Figure 2: SEM image of Au nanocrystals on SiO_2 surface.

Results and Conclusions

After 1.2 nm Au deposition on the tunneling oxide, the minimization of local energy at the Au/SiO_2 interface reshaped the thin film into discontinuous and spherical Au nanocrystals, as shown in the scanning electron microscopy (SEM) image (Figure 2). The diameter of each nanocrystal was about 5 nm.

To measure the memory window, we performed multiple capacitance-voltage (CV) sweeps from inversion to accumulation and back again. The observed hysteresis of the CV curves indicated memory effect through charge storage. Figure 3 represents the memory window obtained from a double-layer C_{60} and Au floating gate.

We then measured the retention time for each configuration, and as demonstrated in Table I, we compared the values to obtain the optimal configuration for a memory device. Based on the results we concluded that double-layer nanocrystal floating gates with C_{60} as the bottom layer and Au as the upper layer would give the best memory device in terms of memory window and retention time. Since mono-dispersed C_{60} has a diameter of about 1 nm, it performed best in blocking back-tunneling of electrons and holes from the upper layer to the channel in this project.

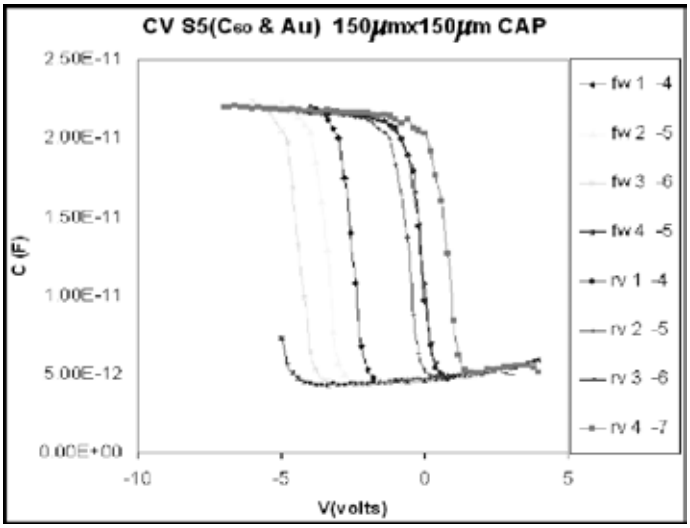

Figure 3: Memory window for a double-layer C_{60}/Au NC memory.

Future Work

More tests will be performed to study the behavior of these memory devices under short-pulse program/erase operations. The retention time will be further improved by incorporating high-κ material as the tunneling dielectric. Finally, the control oxide thickness can be scaled to eliminate short channel effects in the sub-micron gate-length devices.

Acknowledgements

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Run#1 Tunneling oxide = 2.41nm
Run#2 Tunneling oxide = 2.72nm
Voltage sweep (-2 to 5 V)

Sample #	Nanocrystal Layer/s	Run#1		Run#2	
		Mem-win(V)	Reten_t (S)	Mem-win	Reten_t
S1	Control	0	0	0	0
S2	Au	5.8	400	5.4	NA
S3	Au & Au	NA	NA	NA	NA
S4	C60	2.4	240	2.8	250
S5	C60 & Au	3	1100	4.1	5100
S6	C60 & Au	4.7	500	4.4	5000

Table 1: Summary of memory window and retention time.

Simulations of Nano-Particle Electro-Luminescence for Novel Near-Field Microscopy

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Abstract

We simulated two-dimensional electro-luminescence (EL) performances of organic multi-layered quantum dot light emitting diodes (QD-LEDs), through iterative time-step calculations. Simulations were run for LED anode-cathode pairs of various overlapping length. Our simulation results showed that: (1) nearly all recombination happened on the QD mono-layer; (2) when the spatial overlap was zero, the area of emission could be further decreased to 50 nm under driving current densities at the mA/cm^2 level; and (3) with increasing driving current, the decay time of the excitons significantly slow down leading to the saturation of neighboring QDs, and therefore loss in resolution.

Introduction

The resolution of near-field optical signals, captured at a distance shorter than the wavelength of the emitted light, is determined by area of light emission rather than Rayleigh diffraction. Near-field scanning optical microscopes (NSOMs) use this phenomenon on scanning probe microscopes (SPM). Light emitting diodes (LEDs) can be incorporated on the probe tip leading to aperture free NSOMs [1]. We have fabricated a silicon microprobe integrated with a nanometer-sized LED, consisting of organic quantum dots (QD) on the tip, for NSOM. The physical properties of the QD-LED directly define the spectral range and imaging resolution due to the quantum confinement effects.

Methodology

We applied the Poisson equation using the charge distribution to solve the potential which was consequently used to determine charge transport. We then ran a time-step process until steady-state solution was achieved. Quantum tunneling is assumed over nanocrystal energy barriers.

Device Schematic (refer to Figure 1)

The LED was designed to have ohmic electrode contacts, organic transport layers and a monolayer of capped nano-particles. Our two-dimensional simulations varied the lengths of the spatial overlap between the two electrodes. All simulations were done in MATLAB®.

Algorithm Outline

The algorithm basically divided our LED device into many subdivisions. Each subdivision being 10 nm wide and 2 nm tall, which was consequently the resolution of our two-dimensional solution. To decrease run time, we found the smallest device width after which the position-dependent variable distributions did not change significantly. For no spatial overlap, our device was 500 nm.

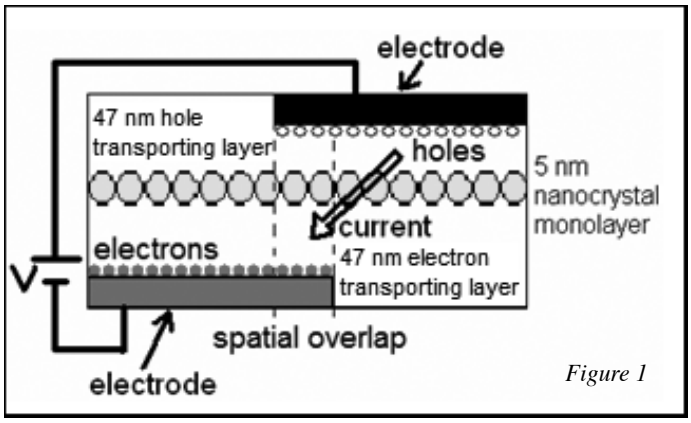


Figure 1

We assumed several variables that were functions of position such as potential, electric field, and carrier transport. Each iteration solved the potential using the charge distribution, and found the new charge distribution from finding charge transport determined from potential. We ran these iterations until the steady state condition [3] was reached:

$$\nabla J_n/q = -\nabla J_p/q = Bnp \qquad (Recombination)\ (1)$$

where the divergence of the current densities over the charge of the carriers, q, was equal to the recombination that occurred at each division. The Langevin recombination constant B was equal to 10^{-18}m^3/sec.

Potential

The potential was determined using the charge distribution by solving the Poisson equation [2]:

$$\nabla^2\Phi = q\,(p-n)/\varepsilon \quad (2)$$

where ε represents the permittivity of free space, p and n represent the hole and electron carrier concentrations and Φ represents the potential. After defining relevant boundary conditions, we numerically solved the potential employing matrices.

Charge Transport

Assuming that carrier injection was due to thermionic emission at the ohmic electrodes, the carrier density at the electrodes was approximated [3] as $10^{24}/m^3$ for holes at the cathode and the electrons at the anode.

We assumed that the charge transport [2] was composed of drift and diffusion:

$$J_p = q(\mu_p pE + D_p \nabla p) \qquad (3)$$

$$J_n = q(\mu_n nE + D_n \nabla n) \qquad (4)$$

where μ represents the mobility variable, D represents the diffusion variable and E represents the electric field. Mobility and diffusion were also functions of position being dependent on electric field [2] as in an electron-hopping like model:

$$\mu_{n/p} = \mu_{0\,n/p} \sqrt{(E/E_{pf})} \qquad (5)$$

$$D = \mu KT/q \qquad (6)$$

where $\mu_{0\,n/p}$ is the mobility constant, and E_{pf} is the activation field related to disorder equal to 10^7 V/m. The mobility constant for each carrier at its respective transport layer was 10^{-10} m^2/Vs and in the other layer as 10^{-12} m^2/Vs [3]. Treating our equations like vectors, we calculated each dimensional component.

Across the nanocrystal monolayer, we found charge flow by taking quantum transmission rates over square wells or barriers using one-dimensional Boltzmann-Maxwellian velocity distributions. The energy diagram was found in previous literature [4] assuming that the transporting layers were PBD, TPD, and the nanocrystals were CdSe.

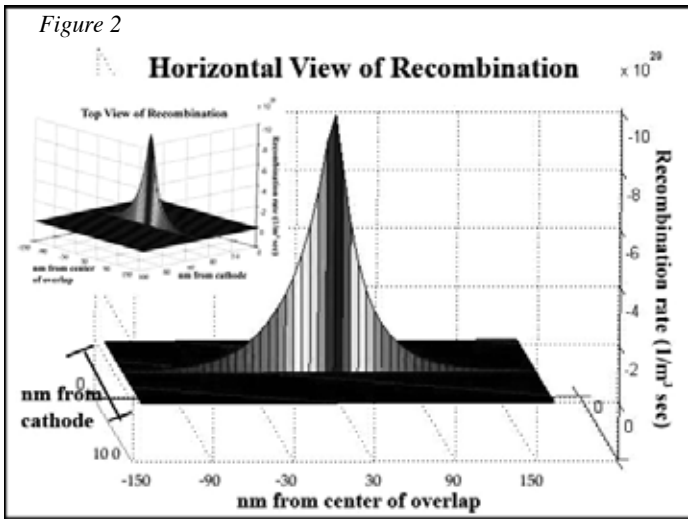
Exciton Kinetics

We assumed that light originated from Forster energy transfers into the nanocrystal monolayer with a slow diffusion limit [5]. We only considered the excitons formed in the nanocrystal monolayer presuming that most of the excitons would form in the monolayer. Because the diffusion coefficient is inversely related to the decay rate squared, τ_{exc}^2, we assumed a modestly long τ_{exc} of 100 ns which would correspond to relatively slow exciton diffusion for CdSe nanocrystals.

Results And Discussion

The recombination profile (see Figure 2) shows that exciton formation occurs only on the nanocrystal monolayer. We expect that since the monolayer is also the most radiative part of the device, the light emission should be easily confined to these nanocrystals. This also verifies our initial assumptions that only the excitons formed on the monolayer are important in computing Forester energy transfers.

Figure 2



Additionally when spatial overlap is zero (see Figure 3), the area of light emission is further confined to 50 nm inside the monolayer at low voltages.

At higher driving currents, the low exciton limit [5], where the exciton injection rate < τ_{exc}^{-1}, is not fulfilled anymore as nanocrystals get more than one exciton (see Figure 4), produced biexcitons and led to slower decay rates. When this happened, there was a loss of resolution implying that the tradeoff for low exciton diffusion was lower light intensities.

Acknowledgements

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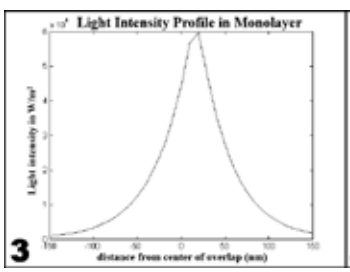

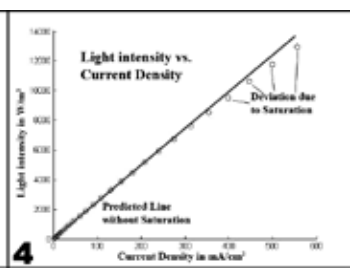

Nanowire-Based Flexible Thin Film Devices

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Abstract

High-performance flexible thin film transistors (TFTs) were fabricated on plastic substrates using lightly tantalum (Ta)-doped tin dioxide (SnO_2) nanowires as the channel material. High densities of crystalline SnO_2 nanowires were dry-transferred directly onto plastic substrates, followed by lithographic patterning of resist, sputtering of chromium/gold (Cr/Au) contacts and a silicon dioxide (SiO_2) insulator layer, and a second lithography process to define a top Cr/Au gate. The top-gated TFT structures exhibit both mechanical flexibility and excellent electrical properties under cyclic tension experiments. Charge carrier mobility was estimated to be as high as 160 $cm^2/(V•s)$—two orders of magnitude higher than that of conventional amorphous-silicon or organic TFTs. The low-cost nanowire growth and dry-transfer processes make this approach a cost-effective means to fabricate flexible TFT's. SnO_2 nanowire-based transparent TFT (TTFT) devices were also fabricated on glass substrates optimized for transparency using sputtered Sn doped indium tin oxide (ITO) electrodes (annealed at 200°C) and a photocured hard-baked epoxy as a gate dielectric (SU8-25 20%, MIBK; Microchem Corp.). Although highly transparent, higher contact resistance was observed for TTFT devices using ITO contacts, additional improvements to these devices need to be further explored.

Introduction

Metal oxide nanowires have attractive electrical and optical properties (i.e. high electron mobility and optical transparency) that make them ideally suited for use in high performance TFTs on low-temperature substrates. In this work, we report on the performance of lightly Ta-doped SnO_2 nanowires incorporated into flexible polyethylene terepthalate (PET) based top-gated TFTs. High density dry transfer of previously synthesized single-crystalline nanowires enables subsequent low-temperature device fabrication without sacrificing device performance [1,2]. The performance of these devices show field effect mobilities in excess of 100 $cm^2/(V•s)$ and on/off ratios > 10^5 which are a marked improvement over existing conventional amorphous-silicon and organic semiconductors [3-5]. Additionally, high optical transmittance of SnO_2 nanowires suggests that TFT devices could be designed for high transparency as well as flexibility [1].

Device Fabrication

Ta-doped SnO_2 nanowires were synthesized with the method described by Dattoli et. al. [1]. After growth, nanowires were dry transferred onto the PET substrate (100 μm thick) in one direction to maximize the number of parallel nanowires (Figure 1, bottom inset). A photolithography process was used to define the Cr/Au source and drain contacts, followed by 360 nm sputter deposition of the SiO_2 gate insulator and definition of the Cr/Au gate contact. All electrical measurements were carried out in air at room temperature.

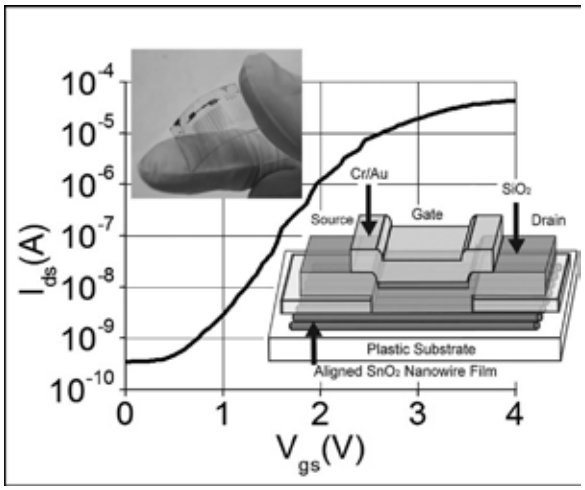

Figure 1: Logarithmic scale gate sweep characteristics of an unbent plastic TFT device shown in the upper inset. Bottom inset depicts the device architecture.

Results and Conclusions

As a result of Ta doping, the TFTs behaved like n-type enhancement-mode transistors [1]. Doping of the SnO_2 nanowires reduced the contact resistance in the TFT devices, evidenced by the ohmic behavior in the linear regime current-voltage (I_{ds}-V_{ds}) characteristics (Figure 2). Devices showed negligible gate leakage at both source and drain. The field-effect mobility, μ_{fe} ranged from 55 $cm^2/(V•s)$ to 160 $cm^2/(V•s)$ and coincided with mobilities measured on similar SnO_2 nanowire-based TTFTs [1]. The mobility was estimated from low-bias (1V) transconductance

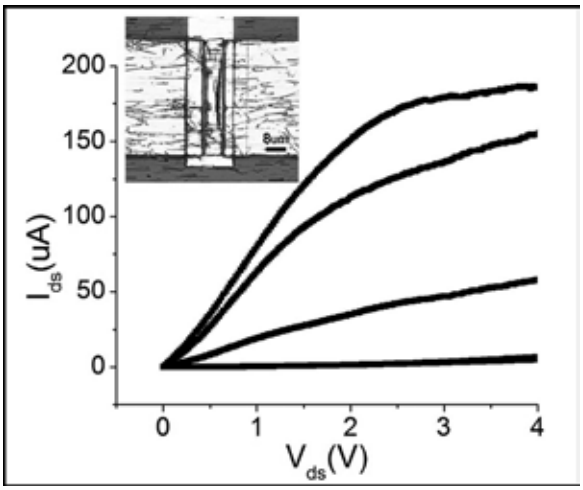

Figure 2: Voltage sweep characteristics of an unbent plastic TFT device shown in the inset.

measurements, and the capacitance of the nanowire "film" was approximated using the formula for an infinite plane ($\varepsilon_0 \bullet 3.9/t_{ox}$) [1]. An on/off ratio of > 10^5 was achieved within a 5V gate bias range with a 1V bias at the source (Figure 1). The channel length and width of this device is 8 μm and 47 μm respectively (Figure 2, inset).

The TFT radius of curvature was used to quantify the degree of compression during bending measurements. The radius of curvature was measured with ImageJ by analyzing photographs of the TFTs during compression (Figure 3). TFTs were tested before and during compression at 8 mm. The gate sweeps in Figure 3 are at a 1V source bias and show high gate mobilities above 100 $cm^2/(V\bullet s)$ for both bent and unbent conditions. This device (Figure 3, lower inset) has a channel length of 3.3 μm and width of 66 μm. At the 8 mm radius of curvature, there is a decrease in the maximum current and ~ 66% reduction in field effect mobility, μ_{fe}.

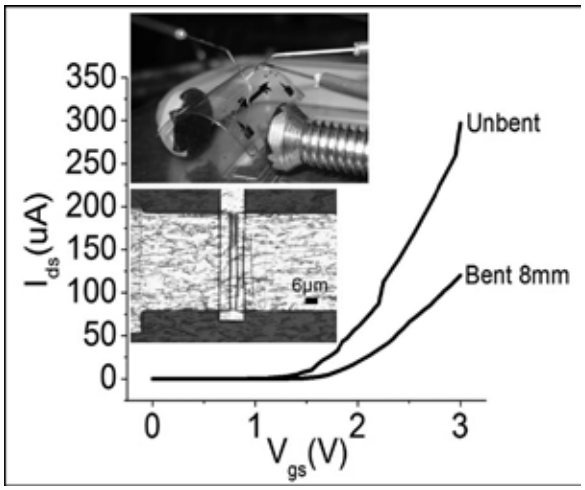

Figure 3: Gate sweep characteristics of an unbent and bent plastic TFT device (insets) taken during compression.

TFT devices were also tested after ten repeated compressions at curvatures from 20 mm to 4 mm. Gate sweeps at decreasing radii of curvature (Figure 4) show μ_{fe} above 100 $cm^2/(V\bullet s)$ and on/off ratios > 10^4. Like devices tested during compression, lower radii of curvatures show an 80% reduction in field effect mobility, and an order of magnitude reduction of the on/off ratio. Even after these reductions, the TFT performance characteristics in compression are still above comparable devices [3-5].

Future Work

The highest fabrication temperature was 150°C which shrank the PET substrate on the order of microns. This shrinkage encumbered alignment of subsequent mask layers. Future processing should maintain temperatures lower than 90°C to minimize plastic substrate shrinkage. Finally, highly transparent TTFT devices using ITO contacts were obtained but showed high contact resistances. Future TTFTs could have thinner SU-8 insulating layers or separate annealing of ITO to minimize sheet resistance prior to spin coating SU-8.

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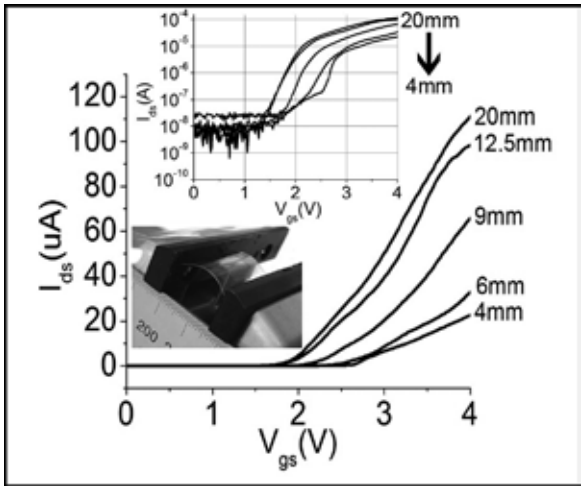

Figure 4: Gate sweep characteristics of the same plastic TFT device tested after 10 compressions of decreasing radius (20-4 mm) shown in the bottom inset. Upper inset shows log scale representation of the same data.

Atomic Layer Deposition on Single/Few Layer Graphene

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Introduction

Due to the limitations of silicon based transistors, as the dimensions are continuously scaled down, there exists the need to find materials that produce more promising electrical properties such as high mobility, nearly ballistic channel and ohmic contact. Carbon based materials, especially single-walled carbon nanotubes (SWNTs), are among the most promising materials thus far. Yet due to the uncontrollability of chirality and position of SWNTs, the large scale integration is still unachievable. Recently, single layer graphene, which is a one atom thick layer of carbon, was discovered to be stable. Due to the structure of graphene, electrons can travel through the material at the same speed, acting as if they have no mass. Graphite, from which graphene is derived, can be grown in a controlled manner leading to the possibility of large-scale integration particularly in the development of field effect transistors. Another unique advantage of graphene materials is their band gap is inversely proportional to the width of the material, as you will see in Figure 1 [1], which indicates that the smaller it is the more potential energy it has, which is a very attractive semiconducting quality. The development and fabrication of such a device however, is nontrivial. Due to graphene being hydrophobic, we must coat the surface of the graphene with a material which will allow for the bonding of the high dielectric material, aluminum oxide (Al_2O_3), serving as the top gate. We used atomic layer deposition (ALD) to deposit the Al_2O_3, and after we coated the graphene, we checked our results using atomic force microscopy (AFM).

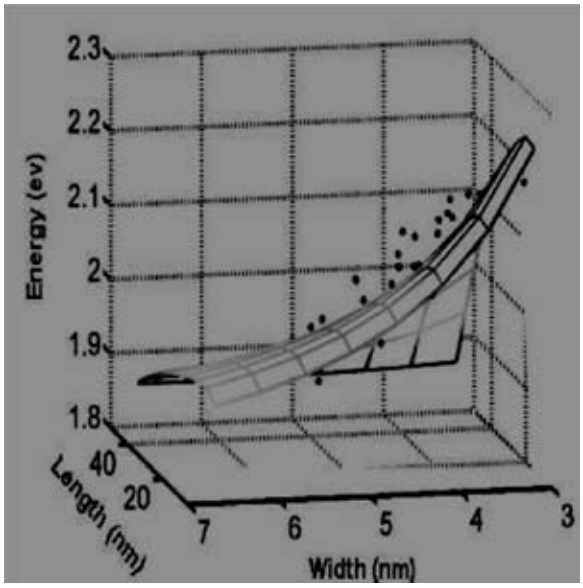

Figure 1: Energy band inversely proportional to the width of the graphene ribbon.

Experimental Procedure

The first stage of our experiment was the development of single layer graphene (SLG). This involved a process named micromechanical cleavage. In this process we cleaved off layers from a $10 \times 10 \times 2$ mm block of highly oriented pyrolytic graphite using scotch tape. Once we achieved relatively thin sheets of graphite on our tape, we contacted the tape against the substrate at varying angles. Next, we investigated our substrate under the 5x/20x optical microscope for signs of graphene which reflects a pale pinkish/purplish color when viewed under the microscope. We proceeded, from this point, by calcining our chip at 470°C for 20 minutes which burned away tape residue and any impurities on the surface. We confirmed our findings using the atomic force microscopy (AFM) system.

Our next step was to deposit the high dielectric oxide layer on the surface. However, since graphene is hydrophobic, we needed to test a control sample, with graphene only, along with a sample soaked for an hour in fluorescein (FITC) and a sample soaked for an hour in deoxyribonucleic acid (DNA), both of which are hydrophilic chemicals. By doing this, we expected the graphene to bond with the high dielectric oxide and uniformly layer over the samples. We proceeded to the atomic layer deposition system, which uses two precursor gases H_2O and tri-methyl aluminum (TMAl). The two gases pulsed respectively and reacted with the surface of the substrate to form the high dielectric, Al_2O_3 (oxide), on the surface. Each cycle put a 0.1 nm layer of Al_2O_3 on the surface and we performed 80 cycles resulting in 8 nm of Al_2O_3. After the ALD was completed, we took more AFM images of our samples to observe and conclude our results.

Results and Conclusions

We were able to conclude from our AFM images that the control sample did have some oxide on the surface however, we were uncertain as to why this would happen because we did not think that any Al_2O_3 would exist on the surface at all. We believe that

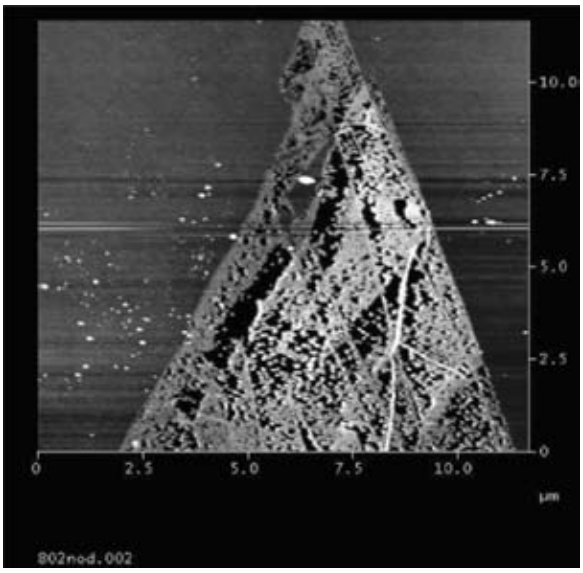

Figure 2: Control sample after ALD.

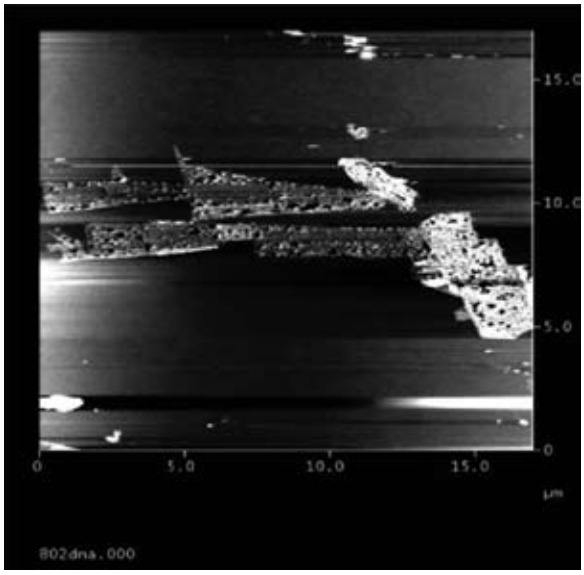

Figure 4: Graphene sample soaked in DNA for one hour after ALD.

this was a result of defects in the graphene. Perhaps the dangling bonds reacted with the Al_2O_3 and caused the dielectric to form. There existed a minimal amount of oxide on the surface, as shown in Figure 2.

We then investigated the sample with the FITC coating and we noticed more Al_2O_3 build up on the surface of the graphene, however it was still not uniformly distributed on the surface as you can see in Figure 3. We also noticed that the Al_2O_3 layer was patterned in blotches which indicated to us that the FITC may have reacted with the graphene forming undesirable bonds.

Lastly, we observed the sample coated with DNA, which had produced the best results thus far. There was considerably more oxide on the surface than both of the previous experiments. The Al_2O_3 was still not uniform over the surface, however, as you can see in Figure 4. We were slightly disappointed by this outcome because our lab had successfully coated carbon nanotubes with DNA in a prior research experiment, so we believed that this would work.

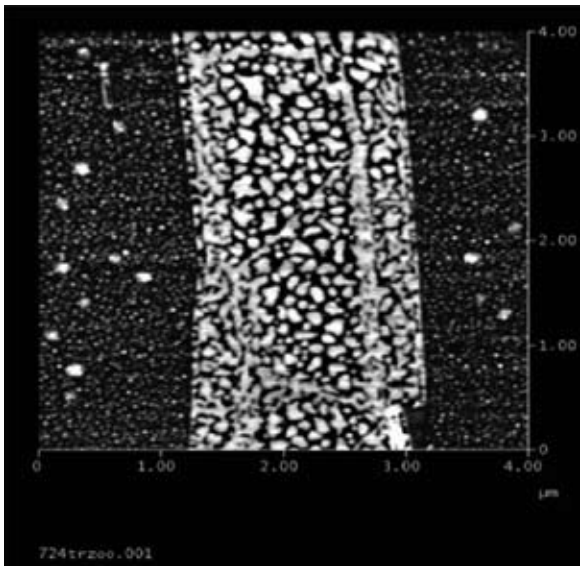

Figure 3: Graphene sample soaked in FITC for one hour after ALD.

Future Work

We will attempt to try more hydrophilic chemicals to achieve a uniform distribution of the Al_2O_3 (oxide) layer. Once achieved, we will etch the graphene down to a narrow ribbon and use the e-beam to pattern contacts on the graphene sample. Once the pattern is made, we will use metal sputtering to deposit the metal contacts on the graphene sample. We will then test the electrical properties of the device and compare with a chemistry method being tested in the lab.

Acknowledgements

I would like to thank my PI, Professor Hongjie Dai, for allowing me the opportunity to work in his lab this summer. I want to acknowledge my mentor Xinran Wang and the Dai Lab for all of their help and effort to help me this summer. I also want to thank Mike Deal and Maureen Baran and the whole Stanford Nanofabrication Facility staff. Last, but certainly not least, I want to thank the Intel Foundation for their financial support, and National Nanotechnology Infrastructure Network Research Experience for Undergraduates Program and Melanie-Claire Mallison for providing this opportunity.

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Carbon Nanotube Transistor Fabrication and Reliability Characterization

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Abstract

Carbon nanotubes (CNT's) are molecular-scale tubes of graphitic carbon with outstanding properties. CNT's are stronger than steel, harder than diamonds, and also posses unique electrical characteristics such as the following: high electrical conductivity, very high tensile strength, highly flexible, high thermal conductivity, and good field emission of electrons. They have the ability to increase the tensile strength and halt crack propagation in concrete, provide stronger yet lighter sports equipment, produce artificial muscles, stronger bridges, are instrumental in production of a space elevator, and act as transistors/diodes/resistors in computer circuits. However, commercial applications have been gradual due to high production costs and issues concerning reliability. When exposed to oxygen or a natural atmosphere, the nanotubes degrade within a few days. Therefore, we suspended CNT's in various polymers which provided a medium that should protect the carbon nanotubes from the atmosphere.

By placing the suspended CNT's on devices that were built on silicon wafers, we were capable of measuring the CNT electrical characteristics. Therefore, we were able to observe how the CNT's degrade with time while being suspended in various polymers. The goal was to discover a polymer that increased the amount of time that CNT's remain effective, and hence greatly enhanced their stability and utilization.

Introduction

The proposed problem is that carbon nanotubes are degrading too quickly in ambient air. Therefore, the point of the study is to experiment with different polymers to passivate the nanotubes and increase their working lifetime. It was hypothesized that carbon nanotubes coated with a polymer will not degrade as quickly as those not coated with polymers. The theoretical implication of the study included the fact that the exact causes of CNT degradation are not known, and the results should determine how the atmosphere changes the quality of the CNT.

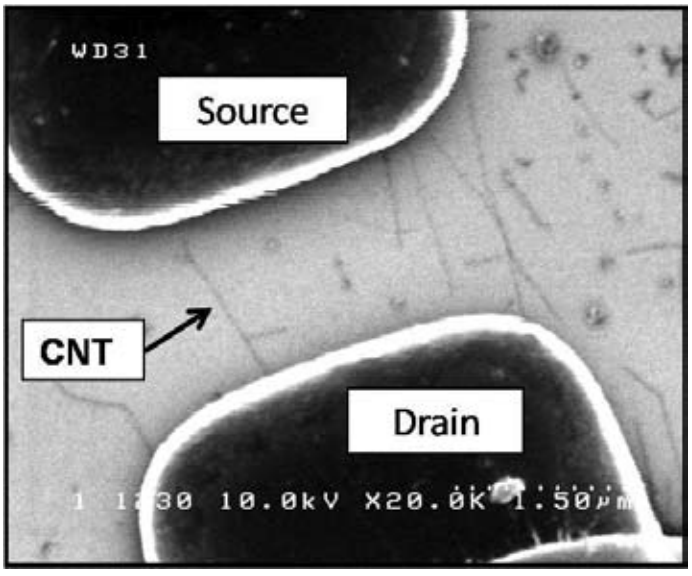

Figure 1: SEM image of CNT connected via the source and drain electrodes on the device.

Experimental Procedures

The experimental design revolved around a plan to build devices, on silicon wafers, which were capable of testing the electrical characteristics of CNT's, and then placing the CNT's on the devices. The CNT's were in the form of a liquid solution which contained completely dispersed CNT's as shown in Figure 1. In order to build the devices and coat them with the polymer, four photolithography steps utilizing different masks were required. Mask one: gold/chrome deposit and liftoff. Mask two: source drain electrodes for CNT. Mask three: isolation to separate devices via gold/chrome etching. Mask four: polymer deposit and polymer etch from bond pad. (Note: The CNT's were deposited using the dielectrophoresis (DEP) method. Experiments were completed to find the etch rate for each polymer, which was removed using the dry etching process.) Figure 2 displays a cross-section of the method for building the device, and the deposition of the CNT's and polymer.

Results

The first run results were flawed due to an issue concerning oxide breakdown, which occurred with those wafers that originally consisted of a 10 nm oxide layer. The calculated

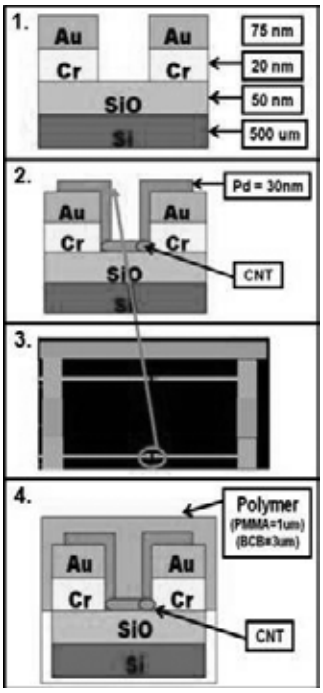

Figure 2: Cross section of four mask method.

voltage breakdown (VB) equaled 100 V. However, the measured VB was 10 V. The remaining runs utilized wafers which consisted of a 50 nm oxide layer which prevented further occurrences of oxide breakdown.

Repeatability test were completed to understand how the probing process may affect the results. One repeatability test showed that when the devices are probed once and a voltage sweep is applied continuously over a set period of time, the results are repeatable. However, the results are not repeatable when the devices are probed multiple times and a voltage sweep is applied each time the device is re-probed. During the first run of the multi-probed repeatability test, the gate and drain current dropped significantly after the eighth device probing was complete.

After the four mask method was complete, the wafer with no polymer had a 69% yield of good devices (see Figure 3), while the wafer covered with polymethyl methacrylate (PMMA) had a 33% yield, and the wafer covered with benzocyclobutene (BCB) had a 7% yield.

A high drain current is desired, because drain current behaves as a conductor. Gate current behaves as an insulator; therefore it needs to be relatively small. The electrical characteristics of the same devices were measured and compared each day to observe the amount of time that elapsed before CNT degradation was noticed (see Figure 4). The CNT's on the wafer without the polymer and the wafer coated with PMMA degraded at

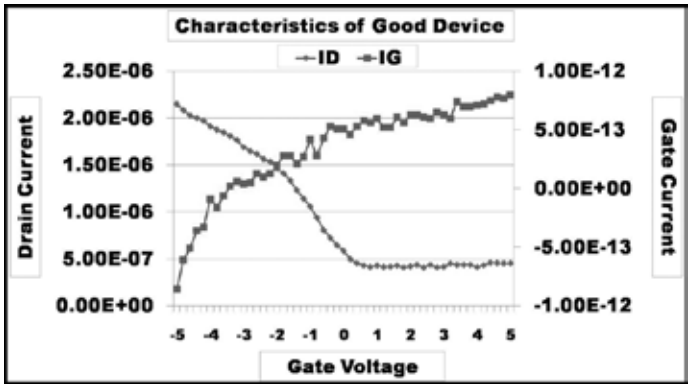

Figure 3: Example of a good semiconductor device.

approximately the same rate. However, on day eight of the experiment, 8% of the devices on the wafer without the polymer remained functional, while 31% of those on the wafer covered with PMMA remained functional. After three days, 0% of the devices on the wafer covered with BCB remained functional.

Conclusion and Future Work

The results led us to conclude that passivation does not appear to improve CNT lifetime, multiple probing appears to degrade the results, and BCB processing degrades CNT yield. The future work involves repeating the experiments with other polymers to observe how the polymers alter the CNT lifetime.

Acknowledgements

The author wishes to thank the National Nanotechnology Infrastructure Network Research Experience for Undergraduates Program, National Science Foundation, Intel Foundation, Deji Akinwade, Dr. Philip Wong, Dr. Noe Lozano, Maria Suggs, Mike Deal, and Maureen Baran.

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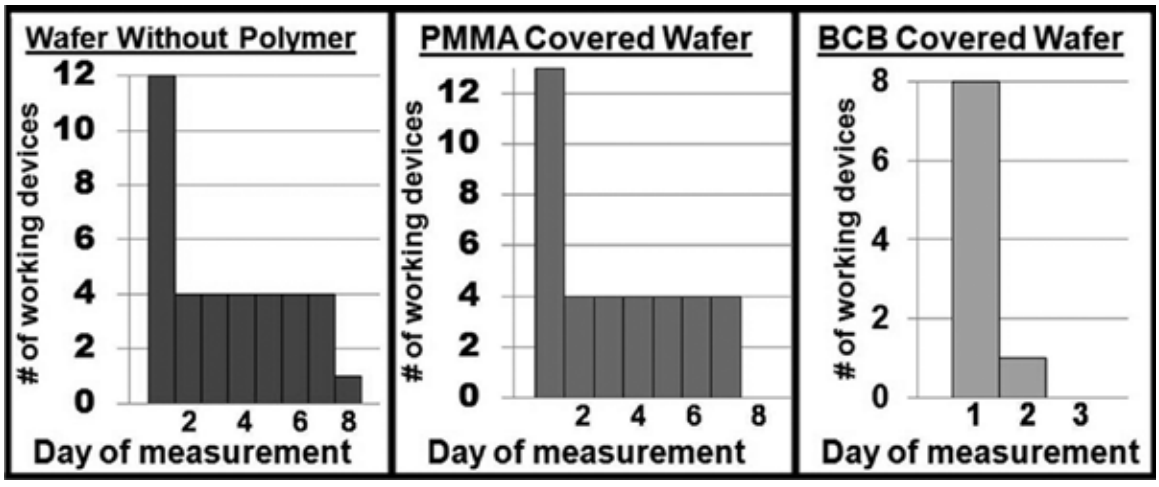

Figure 4: Results of degradation rates for each wafer.

P-Type Contact Optimization in Nonpolar Gallium Nitride-Based Blue Lasers

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Abstract

Polar gallium nitride (GaN)-based blue lasers have been hindered by poor yields in their fabrication. Nonpolar GaN-based blue lasers, which are grown along a different crystal plane than polar GaN-based blue lasers, show great promise for increasing laser yields and lifetimes. They lack the polarized electric field inherent in c-plane GaN substrates. Continuous-wave (CW) operation of nonpolar lasers has been recently achieved, yet they are hindered by their low lifetimes relative to polar blue lasers. Initial measurements suggest that a large increase in lifetime can be realized by reducing the resistance across the p-type metal contacts of the laser. Contacts schemes were tested using a circular transfer length method (CTLM) structures. Significant improvements in the p-type contact resistance have been realized by optimizing metallization schemes, thermal annealing conditions, and doping levels.

Introduction

GaN and related materials have been around for over a decade and are extremely useful blue and near-UV light emitting diodes and lasers. Their uses include ultra high density optical storage, lighting sources, high resolution printing and advanced medical imaging applications [1].

Non-polar GaN substrates are inherently difficult to grow and appropriate metal contacts with work functions higher than p-GaN are difficult to find [2]. The metals are typically more difficult to deposit due to higher evaporation temperatures and consequently are less reliable. Experiments have shown that the majority of the resistance is across the p-type contact resistance, so they are the best candidate for optimization at this point. Typically contacts for polar p-GaN use some combination of platinum (Pt), palladium (Pd), and gold (Au) contacts. Research has also shown that the resistance can be significantly reduced by growing a highly doped, p^{++}, layer on top of the p-GaN just beneath the contacts [2].

Experiment

The p-GaN M-plane substrates were grown by Mitsubishi Chemical. The top 20 nm p^{++} layer was grown by metal-organic chemical vapor deposition techniques. The sample was then rapid thermally annealed at 750°C in nitric oxide (N_2O_2) for 15 minutes. Then 100 nm of silicon oxide (SiO_2) was deposited on top of the p-GaN as a protective layer during processing. The CTLM contacts were fabricated with standard photolithography techniques. The spacing varied between 5 μm to 100 μm. Then we used a 20 minute UV ozone de-scum followed by a 1 minute buffered hydroflouric acid (HF) wet etch and a 30 second hydrochloric acid (HCl) dip. The metal contacts were then put down with standard electron beam deposition techniques. The liftoff was preceded by a 30 second sonication in 70°C deionized water. Depending on what contacts we were making, we would repeat the process to make a set of 100-250 nm gold pads on top of the contacts to protect them during testing. Then I-V curves were obtained for three sets of CTLM's on each sample using a standard 2-probe arrangement. The data was aggregated and the contact resistances were determined at the 250 μA current level.

Results and Discussion

Figure 1 shows the specific contact resistivity as a function of the bis-cyclopentadienylmagnesium (CP_2Mg) flow rate (in standard cubic centimeters). The flow rate of the dopant gas during the metal-organic chemical vapor deposition (MOVCD) process

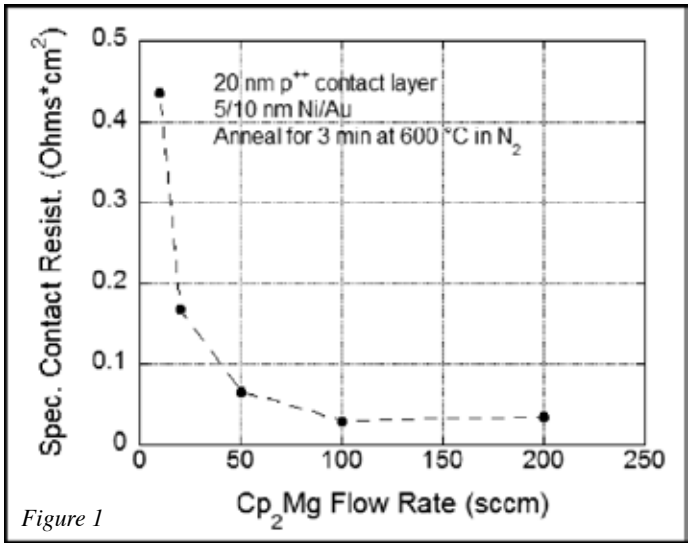

Figure 1

was varied for different samples. 100 sccm was found to be the ideal flow rate. More research is needed to optimize the specific contact resistivity between the 100 and 200 sccm flow rates. With the Ni/Au contacts in the first sample run the I-V curves were found to be considerably non-ohmic, and the resistances and several orders of magnitude higher than the literature on C-plane contacts suggested they should be.

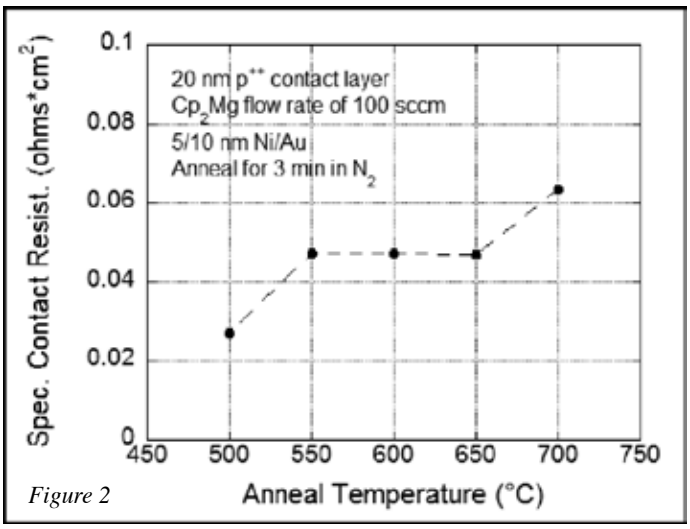

Figure 2

Then the anneal temperature of the Ni/Au contacts themselves was varied (Figure 2). We found considerable difference across the anneal temperatures. We still kept the original anneal temperature for the p-GaN the same for each sample. The overall numbers were around the same order of magnitude as the previous flow series. The I-V curves were slightly more linear, but still far from ohmic. However we determined that the nickel was perhaps not the best metal for the contacts and then varied the metallization scheme for the contacts.

The metallization scheme proved to be our most significant. We found that different metals provided an order of magnitude decrease in contact resistivity. We tried using metals with higher work functions since those seem to have lower contact resistance. The Pt/Pd/Au (7/7/100nm) proved to be the best scheme (Figure 3). Not only was the resistance lower, but most of the I-V curves were nearly perfectly ohmic. At higher spacing the curves were more linear, but at the lower spacing (5 to 10 μm) the curves looked slightly like a p-n junction I-V curve. We later tried several variations of the Pt/Pd/Au scheme and were able to optimize the thickness as well.

Contact Metals	Specific Contact Resistivity (Ω*cm^2)
Pt/Pd/Au	***0.0051***
Ni/Au Annealed in N_2 O_2	0.0106
Ni/Au Annealed in N_2	0.0115
Pd/Au	0.0497
Ti/Au	0.1306

Figure 3

Summary

We found an optimum metal scheme and thickness for the contacts. We also optimized the surface treatments and wet etching processes. Our best contacts were nearly ohmic and the calculated specific contact resistivities were on the order we hoped for. We still have some work to be done with optimizing the flow rate and doping levels of the top p^{++} layer of the p-GaN, but the improvements made so far should give an order of magnitude increase in the laser lifetime and efficiency of the next batch of fabricated lasers.

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I would like to thank the National Nanotechnology Infrastructure Network Research Experience for Undergraduates Program for their funding and support, as well as everyone in the Nakamura research group at UCSB, especially Robert Farrell.

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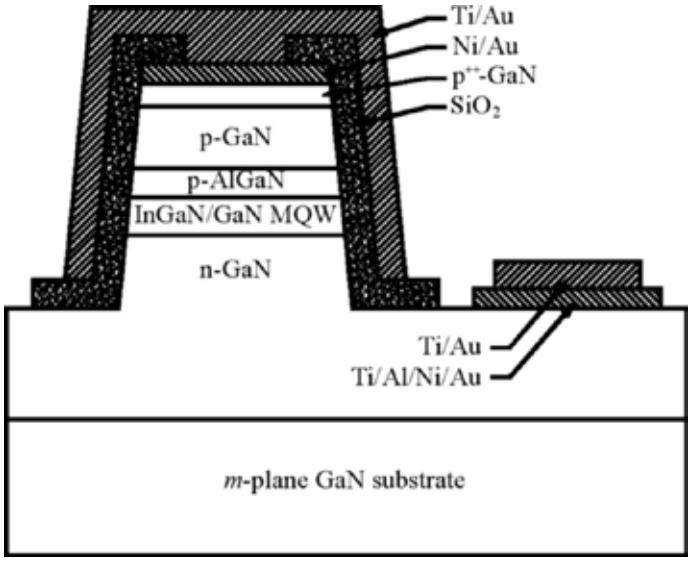

Figure 4: A cross sectional view of the laser [1].

Demonstration of a Novel Fabrication Methodology to Produce Complex, Three Dimensional Structures

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Abstract

Fabrication of high aspect-ratio three-dimensional (3D) microstructures has many important applications in modern microchip technology. A micro-electro-mechanical system (MEMS) fabrication procedure is presented that can produce high aspect-ratio 3D metal structures, which may be used for (but is in no way limited to) electronic, optical, chemical, and/or fluidic interconnection. This represents the interdisciplinary marriage of a number of highly disparate device technologies. The aforementioned MEMS structures were produced through micro-fabrication procedures, including spinning photoresist, post and pre-baking, developing, curing, electroplating, polymer decomposition, and seed layer etching. Some of the applications of the structures which were fabricated using this method include coplanar waveguides, inductors, and microfluidic filters. The primary focus of this research was to develop an enabling process technology to meet the fabrication and integration needs of generic 3D complex device structures.

Introduction

This study was performed in an attempt to demonstrate a novel fabrication methodology for producing complex three-dimensional microstructures. Although this method extends far beyond the creation of high aspect ratio copper pillars, the most comparable previous fabrication methodology was for that purpose.

In the past, there have been many different proposed fabrication methodologies for creating high aspect ratio copper pillars. These included the copper pillar bump process [5,6] and a method involving through silicon vias [2,3,4,6] wherein the silicon is etched following copper filling of the holes (known as "vias").

The pillar bump process involved patterning a layer of photoresist and then electroplating into the resist openings [5,6]. This method was severely limited in several ways, including the fact that it was extremely difficult to electroplate copper into high aspect ratio resist openings and it was very difficult to fabricate high aspect ratio vias in resist [6]. This process, therefore, was typically only able to achieve comparably low aspect ratios (usually, < 5.)

The other process essentially involved creating vias in a silicon wafer and then electroplating into the resultant vias [2,3,4,6]. Via creation was usually done either by etching or laser-ablation [6]. Next, an oxide layer would be deposited onto the wafer, followed by the deposition of a seed layer. The via would be filled with copper through an electroplating process. Finally, the silicon wafer would be etched away (using potassium hydroxide (KOH)) to leave behind the high aspect ratio copper pillars. There were also several problems with this process, to which several solutions were proposed. One such problem was the creation of voids during electro-deposition inside the vias due to the non-uniform current densities resulting from the local geometry of the sample. One proposed solution to this problem was the use of an aspect ratio dependent electro-deposition process, whereby the current density was continuously varied as a function of time [3]. Moreover, it is difficult to bond the resulting pillars to the wafer containing the circuitry.

It has been well established that it is possible to create high aspect ratio polymer pillars [1,7]. These have been mainly been used in attempts to create electrical-optical I/O devices (such as micro-electro-optical-mechanical systems or MEOMS) [1,7].

During a previous REU project, sidewall metallization of polymer pillars for use as chip I/Os was investigated [7], and it was shown to be possible to create copper pillars with aspect ratios exceeding 20:1. Under that method, polymer pillars were created, and then a seed layer was deposited onto them. Once the seed layer had been created, copper was electroplated onto the side wall of the pillar. Finally, the polymer was removed through thermal decomposition. What remained was a high aspect ratio structure [7].

The method proposed here extends that previous work and uses a similar process to create structures with a more complex geometry. Some of the structures created were square spiral inductors, coplanar waveguides, an electromechanical chuck, and a microfluidic filter.

Experimental Procedure

Two different fabrication methodologies were created, capable of creating ~ 50 μm and ~ 140 μm tall polymer pillars respectively (which would directly affect the height of the resulting structures). They differed in that the taller pillars were created by spinning two layers of polymer (Avatrel®) on the substrate surface. Herein, the sample with two layers of Avatrel shall be denoted as being produce through the "2-spin process."

A single layer of Avatrel 2090P polymer photoresist was spun on a silicon dioxide coated silicon wafer at 600 RPM for 40 seconds (twice for the 2-spin process.) The wafer was then pre-baked for 45 minutes on a hot plate at 108°C. Then the wafer was exposed for 25 seconds in an EVG620 mask aligner (50 seconds for the 2-spin). Following the exposure, the wafer was post baked for 20 minutes at 108°C in an oven. The wafer was then developed using an Avatrel development solution. Following this development, the wafer was inserted into a PlasmaTherm reactive ion etcher (RIE) for a minimum of 3 minutes for descumming. After the descum, the wafer was cured in the Lindberg furnace at a temperature of 160°C for 2 hours. After having been cured, the wafer was metallized using the Unifilm sputterer (with 300Å of titanium, 3000Å of copper, and 300Å of titanium). This thin layer of metal acted as a seed layer for the copper electroplating which would occur later in the procedure.

A second layer of Avatrel was then spun on top of the wafer, again at 600 RPM for 40 seconds (this is done twice for the 2-spin process.) The wafer was then pre-baked once more, and then exposed using the mask aligner (for 30 seconds for the single spin process and 37 seconds for the 2-spin process). Once again, the wafer was post baked at 108°C for 20 minutes, following which the wafer was again developed. The wafer was placed into the RIE for a minimum of an additional 3 minutes. The wafer was then placed into a buffered oxide etchant (BOE) to remove the 300Å layer of titanium on its surface. The top surface of the wafer was then electroplated using a copper sulfate solution, a copper anode and the wafer as the cathode. The wafer was then thermally decomposed in the Lindberg Furnace for 2 hours at 450°C to remove the Avatrel. To remove the remaining seed layer, the wafer was placed into a copper etching solution produced from a 1:1 ratio of hydrogen peroxide and ammonium peroxide.

Results and Conclusions

A novel fabrication methodology for producing complex, 3D structures was demonstrated to be feasible. Several different structures with various different interdisciplinary applications were constructed. In addition, process optimization has been performed. An aspect ratio of ~ 17.1:1 was achieved, as measured via images from the Hitachi scanning electron microscopy (SEM).

Future Work

In the future, additional work can be done on building taller structures, or structures with more complex geometries. Work can also be done on providing a computational model of the various stresses, strains, and forces induced on the structures to determine the origins (and theoretical magnitudes) of the several different kinds of deformations that were observed to occur on the structures during the fabrication process.

Acknowledgments

The author would like to thank the National Science Foundation and, in particular, the National Nanotechnology Infrastructure Network, for allowing me to be involved in this REU program. Gratitude should also be extended to the Georgia Institute of Technology, the Microelectronics Research Center (MiRC) and its staff, and, in addition to the author's mentor, Hang Chen, and principal investigator, Muhannad Bakir. Likewise appreciation should be extended to Mrs. Jennifer Tatham Root and her assistants. Finally, acknowledgment needs to be given to Dr. James Meindl.

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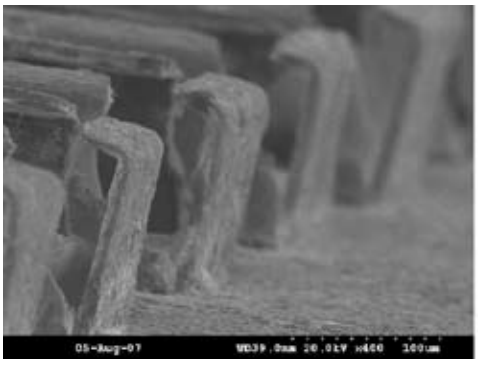

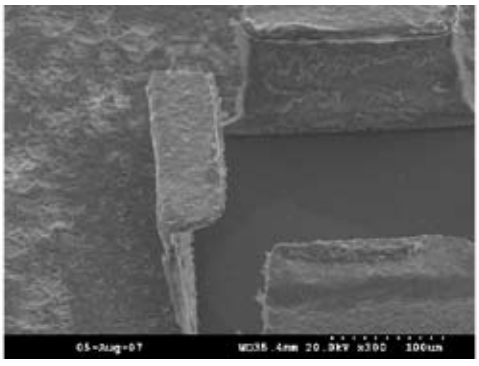

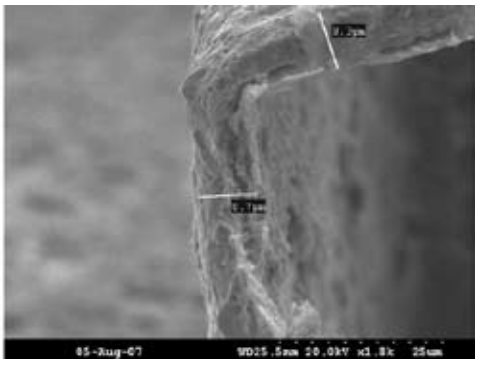

Adhesion and Electromigration Performance of Barrier / Copper Interconnections in CMOS Technologies

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Introduction and Motivation

Electromigration (EM), the movement of metal atoms due to the flow of current, can cause failure in interconnects in complementary metal oxide semiconductor (CMOS) circuits. EM performance in copper (Cu) interconnect structures is largely related to the diffusion of copper atoms along the barrier layer interfaces. It has been shown that the mobility of copper atoms is closely related to the adhesive strength of this copper / barrier layer interface [1]. In the past these properties have usually been assessed separately.

Previously, Zhou et al. [2] reported that there was an increase in electromigration mean-time-to-failure as the interlayer adhesion increased. Lane et al. [1] showed that when the interface debonding energy of a copper / barrier layer is small, the void growth rate during EM is higher. This is presumably due to more mobile copper atoms. This again shows a connection between EM and adhesion.

In our work, we are developing a novel technique for characterizing EM performance and adhesion of a copper/barrier layer simultaneously. Once this technique is developed, it will provide a unique tool in optimizing EM performance in the next generation of integrated circuits and nanoelectronics. Using thin film fracture mechanics techniques, adhesion in copper / barrier film stacks was analyzed in the presence of electromigraton. The crack propagation rate or velocity, v, was measured versus applied strain release rate, G (which is a measure of adhesion). This was measured while different current densities were applied. X-ray photoelectron spectroscopy (XPS) was performed on the fracture surfaces to see if the failure does indeed occur at the Cu/barrier interface.

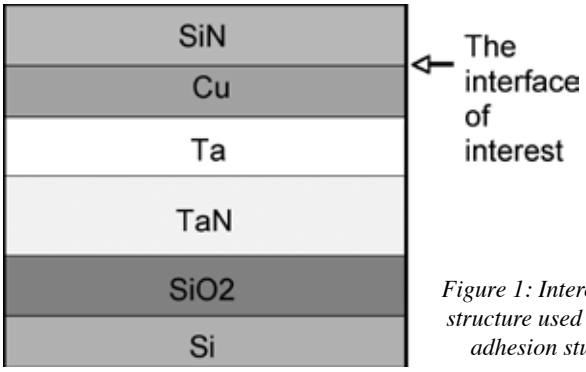

Figure 1: Interconnect structure used in EM/ adhesion studies

Experimental Method

Samples were obtained of typical multilayer interconnect structures, as shown in Figure 1. Copper was the main conducting layer and silicon nitride (SiN) was the barrier layer on top. The SiN layer was etched off at the ends in order to make contact areas. 85% aqueous phosphoric acid at room temperature was used. The resistance was measured every 5 minutes until the SiN was removed.

As shown in the schematic diagram in Figure 2, the crack propagation rate or velocity, v, was measured versus applied strain release rate, G (which is a measure of adhesion) by using standard subcritical double-cantilever beam fracture mechanics method. This was measured while different current densities were applied.

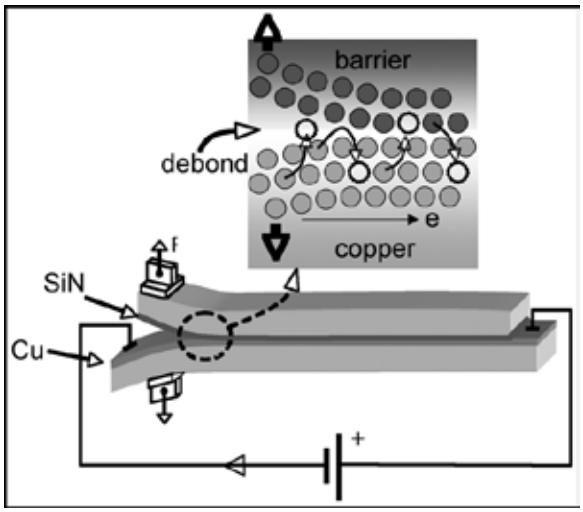

Figure 2: Schematic of samples used in standard subcritical double-cantilever beam fracture mechanics measurement, to measure crack velocity, v, versus adhesion, G, for different current densities.

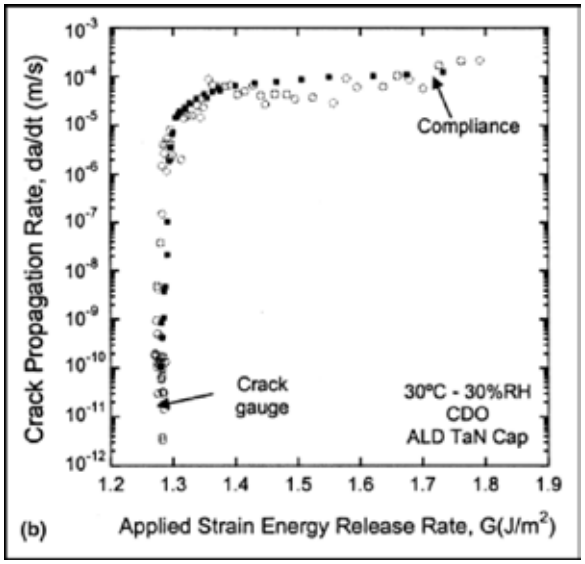

Figure 3: Previous results of our group measuring crack velocity versus adhesion without any current [3].

Results and Discussion

Figure 3 shows the results of previous work by our group [3]. This shows the relationship between crack velocity, v, versus the applied strain energy release rate, G (or driving force for cracking/debonding) for a copper/tantalum nitride interconnect without any current. In our present results, shown in Figure 4, we see v-G curves for two control specimens and two specimens with different current flow, J. Negative J represents electrons flowing opposite to the crack growth direction and positive J represents electrons flowing along the crack growth direction. We can see that these current densities are ~ 2 orders of magnitude below those used in standard electromigration tests, and there is no noticeable effect on crack growth at these low current densities.

XPS was done on the two surfaces exposed by the fracture in order to determine which interface of the structure failed. Table 1a shows XPS results of the top fracture surface (in Figure 2), indicating it is indeed a SiN layer. Table 1b shows XPS results of the bottom fracture surface (in Figure 2), indicating it is, in fact, a copper layer. From these results, we can conclude that the crack is indeed growing between the layer of Cu and the layer of SiN.

Si (2s)	34.6 %
N (1s)	24.1 %
Cu (3p)	0.5%
O (1s)	28.4 %
C (1s)	12.4 %

Cu (3p)	28.7 %
O (1s)	45.0 %
C (1s)	26.3 %

Conclusions

Using thin film fracture mechanics techniques, adhesion in copper / barrier film stacks was analyzed in the presence of electromigraton. Initial results at low current densities show no change in adhesion. X-ray photoelectron spectroscopy was performed on the fracture surfaces to show that the failure does occur at the Cu/barrier interface. Further measurements of crack propagation at higher current densities need to be done. Challenges that need to be overcome in the future are excessive Joule heating at these higher current densities, and enhanced oxidation for Cu and failure of solder joints at the higher temperatures due to the Joule heating.

Acknowledgments

I would like to thank Prof. Dauskardt for letting me work in his group, Michael Deal for being so helpful and for guiding me through the process, and Ryan Birringer for mentoring me, helping me out throughout the experiments and for answering all of my questions. Also I would like to thank the National Nanotechnology Infrastructure Network Research Experience for Undergraduates Program, CIS, and NSF for giving me this opportunity.

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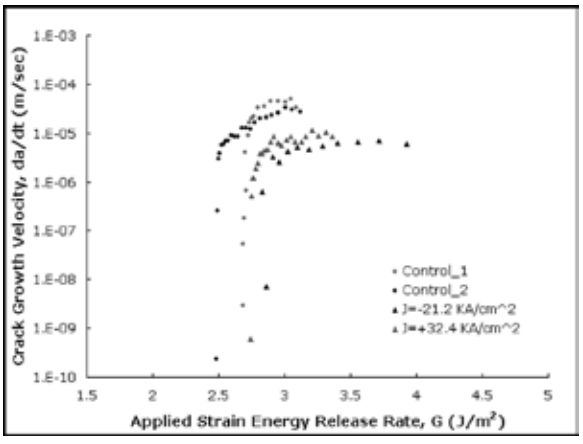

Figure 4, above: v-G curves for this work for two current densities, showing little effect on crack growth.

Table 1a, top left: XPS results of the bottom fracture surface (in Figure 2), indicating a copper layer.

Table 1b, bottom left: XPS results of the top fracture surface (in Figure 2), indicating an SiN layer.

Post-22 Nanometer Non-Classical CMOS Transistors

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Abstract

As silicon transistors are reaching their limits, next-generation complementary metal oxide semiconductor (CMOS) transistors may use new materials such as III-V's (i.e. indium gallium arsenide (InGaAs)). Key steps in new transistor fabrication include epitaxial regrowth, planarization, and etchback. Several planarization materials have been tested to develop a smooth and controllable protection layer during gate exposure.

Introduction

Moore's Law predicts the doubling in transistor surface area density roughly every two years. However, silicon is rapidly approaching its limit in scalability, which will require fabrication with new semiconductor materials. Currently, 65 nm gate length silicon devices are on the market, with 45 nm devices following behind. It is believed that silicon can be scaled to 22 nm devices, but beyond this limit, more exotic III-V materials such as InGaAs may be used in CMOS fabrication, which introduces a host of new engineering challenges.

The group objectives are to demonstrate a concept device showing that CMOS transistors can be reliably fabricated using III-V materials, confirm the record breaking current density of greater than 6 mA/μm that theory predicts, and then scale to sub-22 nm gate lengths.

A crucial aspect of the fabrication routine is the planarization process, whereby the source/drain contact regions are protected when the gate stack is exposed. Once the gate stack has been processed, a highly-doped InGaAs layer is conformally regrown across the wafer to provide current carriers, followed by a molybdenum (Mo) layer for ohmic contacts. These layers must be etched off the top of the gate stack, yet remain intact on the source/drain contact regions. However, the physical and chemical etch processes not only penetrate the source and drain regions, but they are also capable of damaging the InGaAs conduction channel, as shown in Figure 1.

In the planarization process, a thick layer of material is spun on a wafer to create a smooth plane at the surface. This layer is then ashed back to just below the gate height, exposing the gate but covering the source/drain regions. The InGaAs and Mo layers are then removed from the gate stack, and stripper solution removes the remaining planarization material from the source/drain regions so that contacts can be laid.

Experimental Procedure

Three different potential planarization materials were tested for the smoothest, most reliable, and most controllable characteristics: SPR510, a photoresist; PMGI SF11, a photoresist underlayer material; BCB, a plastic material.

The three planarization materials differed in their spin and curing recipes, as well as the ash process. PMGI is ashed back with MIF701 developer, SPR510 with an O_2 plasma, and BCB with CF_4/O_2 plasma. During the ash stages, samples were progressively cleaved and inspected in the scanning electron microscope (SEM) to check the planarization height relative to the gate stacks. Once they were ashed to the proper height, the Mo and InGaAs etches were performed to see if the planarization materials provided proper protection.

All materials were tested on samples that contained "pseudo" gate stacks, which were composed of chromium (Cr) and silicon dioxide (SiO_2) on a Si wafer, and differ from the final design depicted in Figure 1. The entire sample was then covered in Mo to simulate the regrowth stage.

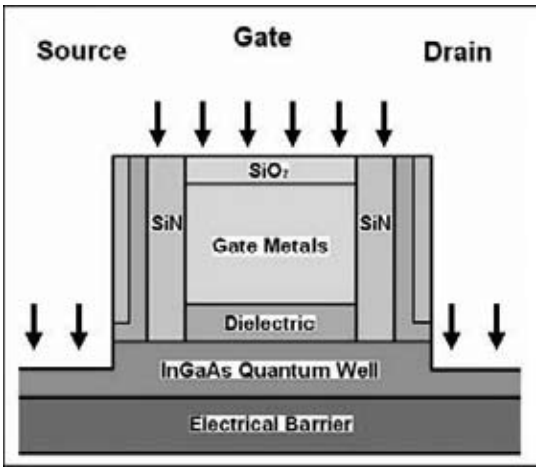

Figure 1: Mo and InGaAs etching can damage conduction channel.

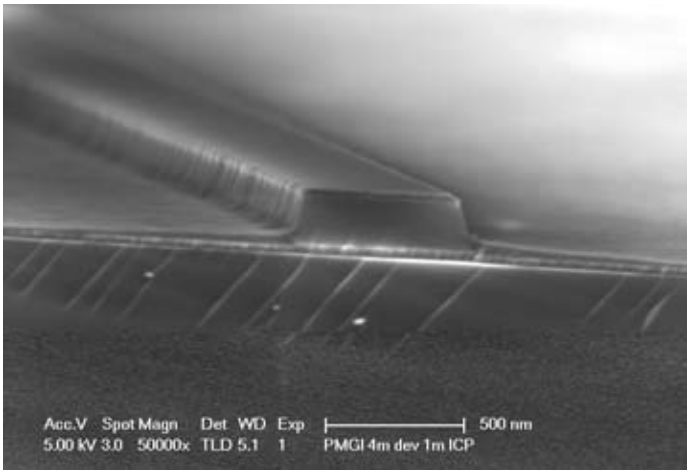

Figure 2: PMGI sample after developing and Mo etch.

Results and Conclusions

PMGI SF11 developed smoothly and evenly, creating the desired planar surface. However, it was difficult to spin on a smooth layer, and the PMGI etched off very rapidly under the Mo etch. As seen in Figure 2, almost no PMGI remains on the surface, so the source/drain regions are exposed.

The BCB samples maintained a smooth surface just below the gate height after ashing, but BCB requires a sensitive curing process, is difficult to remove, and takes much longer to process than SPR510, so it is being saved as a backup option in the final process.

SPR510 spins on smoothly and the ash rate is much slower and thus more controllable. However, when ashed with O_2 plasma, the surface was very rough and it was difficult to obtain a smooth gate stack exposure. Experiments were also executed with a post-ash reflow bake and O_3 plasma to smooth the surface, but these processes yielded little improvement—if any—on the surface roughness, as seen in Figure 3.

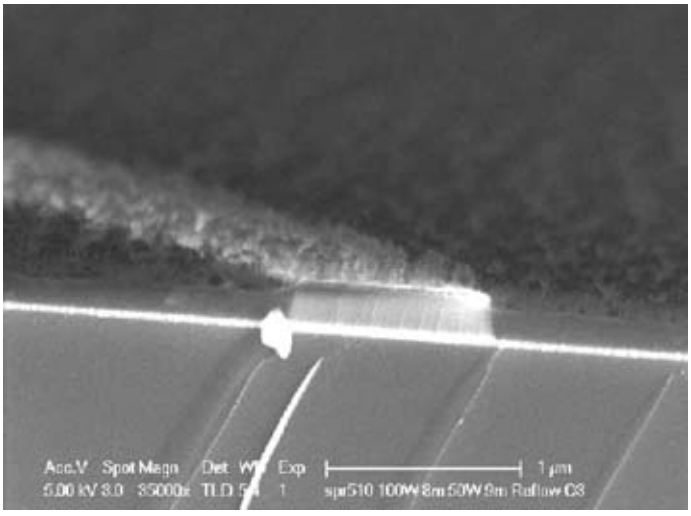

Figure 3: SPR510 after ash, reflow bake, and O_3 plasma.

It was later suggested that ashing the SPR510 in inductively-coupled plasma (ICP) rather than the capacitively-coupled plasma may yield a smoother surface. As seen in Figure 4, the sample has a much smoother surface, a cleanly exposed gate following the Mo etch, and most of the original photoresist remains at the level of the gate stack.

Each of the three materials has distinct strengths and weaknesses, but SPR510 appears to be the best candidate for the planarization process. It yields a smooth surface, controllable ash rate, and withstands the subsequent Mo and InGaAs etches. PMGI etches too rapidly, and BCB may be a strong candidate, but is much more cumbersome to work with than SPR510.

Future Work

The team must integrate the three distinct stages of the entire transistor fabrication process. The planarization process has been developed using gate stacks that mimic the samples that will be returned from the regrowth lab. The process must be fine-tuned from beginning to end with the gate stack fabrication, regrowth layers, and planarization process, as well as back-end processing.

Acknowledgements

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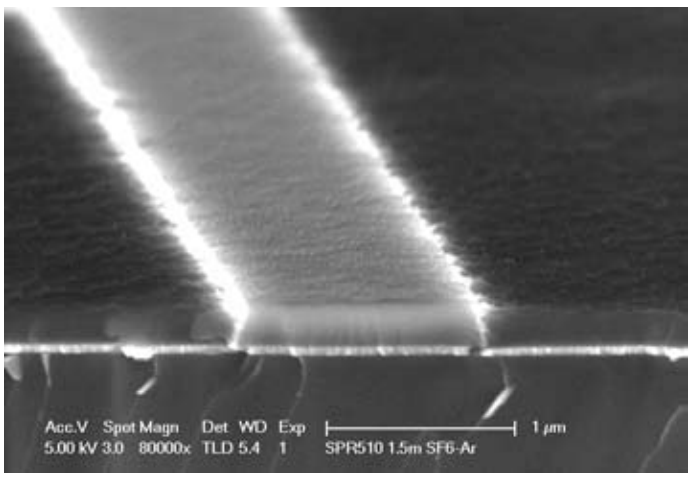

Figure 4: SPR510 after ICP and Mo etch.