Patterning of Electrical Circuits on Fluidic Assembly Microtiles

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Abstract

As an alternative to pick-and-place assembly techniques, recent research has lead to the development of microelectro-mechanical systems (MEMS) components that assemble spontaneously in fluid [1-3]. These efforts have relied heavily on surface-energy minimization and therefore work best when components are assembled by vertical stacking to obtain a product with multiple layers. Our research provides an alternative method for interfacing MEMS components assembled in fluid, which involves horizontal (in-plane) assembly. Our previous work has produced silicon microtiles with mechanical latches that can be manipulated by controlling local fluidic forces in a microchamber [4]. The goal of this research was to demonstrate electrical connection between tiles in a single plane. This was achieved by patterning tiles with gold electrodes so that their tops and sidewalls had a continuous covering of conductive material. The result of this research is a novel method for the electrical interfacing of fluidically-assembled MEMS components.

Background

Past research includes fabrication and testing a series of latching silicon microtiles of varying sizes that can be controlled and assembled in a microfluidic channel. The microtiles are manipulated by controlling the fluid flow through a polydimethylsiloxane (PDMS) microchamber with off-chip valving. The tiles are fabricated from a silicon-on-insulator (SOI) wafer using photolithography and a deep ion etch through the top silicon layer, then released from the wafer by etching the oxide using a 49% hydrofluoric acid (HF) solution.

Fabrication

We developed a fabrication method to pattern gold electrodes on 500 μm square by 30 μm high silicon microtiles. Electrode fabrication began prior to HF release, and included evaporation followed by photolithography processes, finally leading to a chemical etch of the metal to form electrodes on the tops and sides of tiles. A wet etch was chosen instead of a lift-off technique to avoid leaving unwanted metal in the trenches between the etched tiles. The consequence of residual metal between tiles would have been either damage to electrodes or no tile separation after release, both results rendering our tiles useless for in-plane fluidic assembly.

Because gold is reluctant to adhere to silicon, a 15 nm chromium adhesion layer was deposited using an electron-gun evaporator, followed by the 80 nm gold layer. After evaporation a thick (35-40 μm) layer of AZ-4903 positive-tone photoresist was spun to cover and fill the gaps between tiles. The resist was removed around electrodes using a two-step exposure and development process (Figure 1). The first exposure patterned the electrodes on the tiles.

During the first development it was necessary to under-develop the electrode pattern, with the purpose of leaving some resist to be removed during the second development. During the second exposure, the trenches between tiles were heavily exposed. A second development removed all resist between the tiles, leaving only sidewall coverage as required for the electrical connections between tiles. A wet etch of both gold and chromium removed all unwanted metal from the silicon.

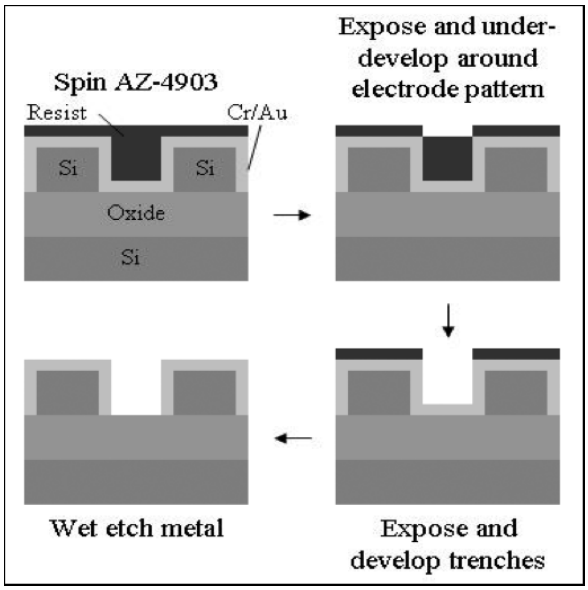

Figure 1: Diagram of two-step exposure and development process for patterning electrodes.

Without this two-step exposure and development process, we experienced either residual photoresist in the trenches between the tiles or overexposure/overdevelopment of the electrodes on the tiles. Finally, tiles were released using 49% HF solution.

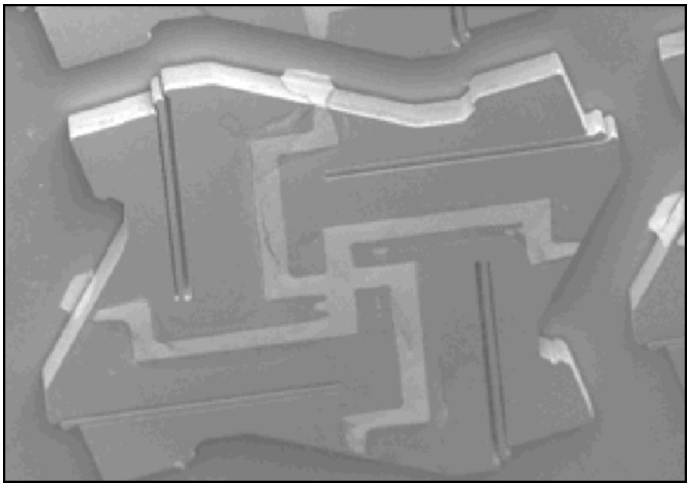

Figure 2: Scanning electron microscopy (SEM) image of silicon tile and gold electrode pattern.

Results

Our fabrication yielded many tiles suitable for electrical testing (Figure 2), though inconsistencies with the electrode pattern did arise, likely caused by variable resist thickness due to edge effects while spinning AZ-4903. Electrical testing using a multimeter probe station verified connectivity across one, two and three-tile circuits assembled in silicone oil on a glass substrate (Figure 3). The tiles were manipulated and assembled using the probe tips (Figure 4).

When compared to similar tests using a non-patterned silicon tile control, electrode-covered tiles yielded a circuit resistance four orders of magnitude smaller. To further characterize our resistance results, we used $R = \rho L/A$ to theoretically calculate circuit resistance, R (Ω). We calculated the theoretical resistance across one tile with chromium and gold wires in parallel to be 4 ohms. Since this value is much smaller than the measured resistances, we assumed that electrode resistance is negligible compared to contact resistances at the tile-tile and probe-tile interfaces. Using this assumption and a least-squares regression, the contact resistances at tile interfaces and for each probe are 880 Ω (0.00792 Ω-cm^2) and 280 Ω respectively.

Conclusion

We fabricated and tested 500 × 500 × 30 μm silicon microtiles patterned with gold electrodes capable of assembling in fluid to form mechanical structures with in-plane electrical connections. By obtaining resistance data across one, two, and three tile circuits, we have verified electrical conductivity across tiles. The results indicate that electrical conduction occurred through planar assemblies of electrode-patterned tiles. Therefore, our fabrication method is capable of producing planar MEMS assembled from individual, microscale components.

Future Work

With the development of our fabrication process, it is possible to obtain simple electric connections between silicon microtiles attached in-plane. Further research will fabricate more complex circuit elements on individual microtiles, enhancing the functionality of systems built from these components.

Acknowledgements

I would like to thank the National Science Foundation as well as the National Nanotechnology Infrastructure Network REU Program for their support of this research. I would especially like to thank Mike Tolley, Mekala Krishnan, Dr. David Erickson and Dr. Hod Lipson, the Erickson Lab as well as the entire Cornell NanoScale Facility staff for their professional help and guidance on this project. Lastly, I would like to thank Dr. Garcia at Cornell for the use of his probe station.

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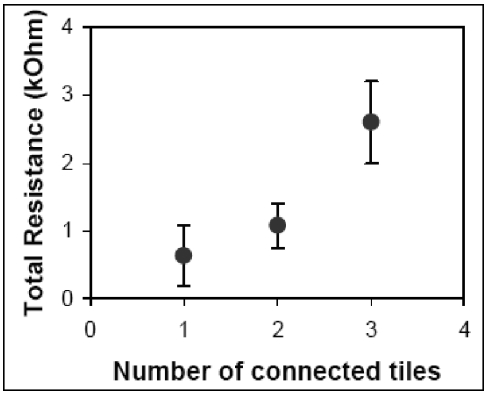

Figure 3: Resistance measurement verses number of tiles. Data points are average measured values. Error bars are minimum and maximum values.

Figure 4: Optical microscope image of resistance measurement across three assembled microtiles.