Post-22 Nanometer Non-Classical CMOS Transistors

Austin Nelson

Electrical Engineering and Physics, University of St. Thomas

NNIN REU Site: Nanotech—The UCSB Nanofabrication Facility, University of California, Santa Barbara
NNIN REU Principal Investigator: Dr. Mark Rodwell, Electrical and Computer Engr., University of California, Santa Barbara
NNIN REU Mentor: Gregory Burek, Electrical and Computer Engineering, University of California, Santa Barbara
Contact: aanelson@stthomas.edu, rodwell@ece.ucsb.edu, burek@ece.ucsb.edu

Abstract

As silicon transistors are reaching their limits, next-generation complementary metal oxide semiconductor (CMOS) transistors may use new materials such as III-V's (i.e. indium gallium arsenide (InGaAs)). Key steps in new transistor fabrication include epitaxial regrowth, planarization, and etchback. Several planarization materials have been tested to develop a smooth and controllable protection layer during gate exposure.

Introduction

Moore's Law predicts the doubling in transistor surface area density roughly every two years. However, silicon is rapidly approaching its limit in scalability, which will require fabrication with new semiconductor materials. Currently, 65 nm gate length silicon devices are on the market, with 45 nm devices following behind. It is believed that silicon can be scaled to 22 nm devices, but beyond this limit, more exotic III-V materials such as InGaAs may be used in CMOS fabrication, which introduces a host of new engineering challenges.

The group objectives are to demonstrate a concept device showing that CMOS transistors can be reliably fabricated using III-V materials, confirm the record breaking current density of greater than 6 mA/μm that theory predicts, and then scale to sub-22 nm gate lengths.

A crucial aspect of the fabrication routine is the planarization process, whereby the source/drain contact regions are protected when the gate stack is exposed. Once the gate stack has been processed, a highly-doped InGaAs layer is conformally regrown across the wafer to provide current carriers, followed by a molybdenum (Mo) layer for ohmic contacts. These layers must be etched off the top of the gate stack, yet remain intact on the source/drain contact regions. However, the physical and chemical etch processes not only penetrate the source and drain regions, but they are also capable of damaging the InGaAs conduction channel, as shown in Figure 1.

In the planarization process, a thick layer of material is spun on a wafer to create a smooth plane at the surface. This layer is then ashed back to just below the gate height, exposing the gate but covering the source/drain regions. The InGaAs and Mo layers are then removed from the gate stack, and stripper solution removes the remaining planarization material from the source/drain regions so that contacts can be laid.

Experimental Procedure

Three different potential planarization materials were tested for the smoothest, most reliable, and most controllable characteristics: SPR510, a photoresist; PMGI SF11, a photoresist underlayer material; BCB, a plastic material.

The three planarization materials differed in their spin and curing recipes, as well as the ash process. PMGI is ashed back with MIF701 developer, SPR510 with an O_2 plasma, and BCB with CF_4/O_2 plasma. During the ash stages, samples were progressively cleaved and inspected in the scanning electron microscope (SEM) to check the planarization height relative to the gate stacks. Once they were ashed to the proper height, the Mo and InGaAs etches were performed to see if the planarization materials provided proper protection.

All materials were tested on samples that contained "pseudo" gate stacks, which were composed of chromium (Cr) and silicon dioxide (SiO_2) on a Si wafer, and differ from the final design depicted in Figure 1. The entire sample was then covered in Mo to simulate the regrowth stage.

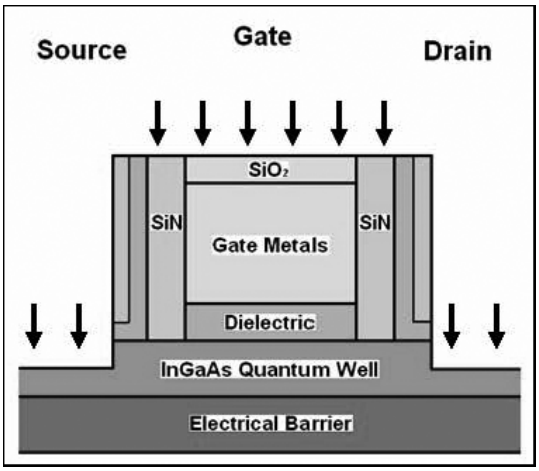

Figure 1: Mo and InGaAs etching can damage conduction channel.

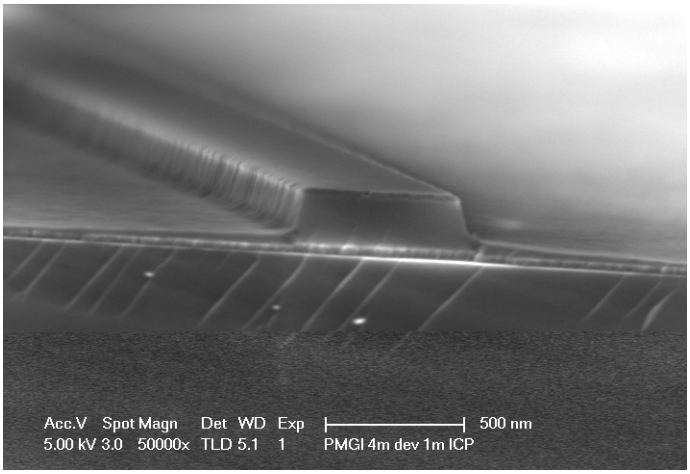

Figure 2: PMGI sample after developing and Mo etch.

Results and Conclusions

PMGI SF11 developed smoothly and evenly, creating the desired planar surface. However, it was difficult to spin on a smooth layer, and the PMGI etched off very rapidly under the Mo etch. As seen in Figure 2, almost no PMGI remains on the surface, so the source/drain regions are exposed.

The BCB samples maintained a smooth surface just below the gate height after ashing, but BCB requires a sensitive curing process, is difficult to remove, and takes much longer to process than SPR510, so it is being saved as a backup option in the final process.

SPR510 spins on smoothly and the ash rate is much slower and thus more controllable. However, when ashed with O_2 plasma, the surface was very rough and it was difficult to obtain a smooth gate stack exposure. Experiments were also executed with a post-ash reflow bake and O_3 plasma to smooth the surface, but these processes yielded little improvement—if any—on the surface roughness, as seen in Figure 3.

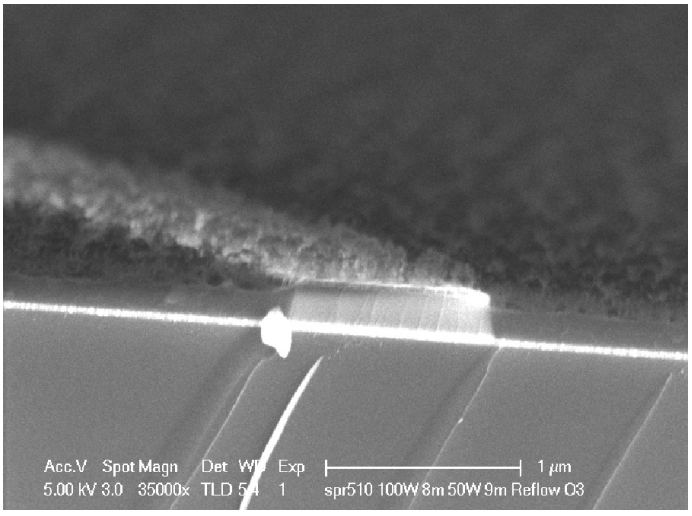

Figure 3: SPR510 after ash, reflow bake, and O_3 plasma.

It was later suggested that ashing the SPR510 in inductively-coupled plasma (ICP) rather than the capacitively-coupled plasma may yield a smoother surface. As seen in Figure 4, the sample has a much smoother surface, a cleanly exposed gate following the Mo etch, and most of the original photoresist remains at the level of the gate stack.

Each of the three materials has distinct strengths and weaknesses, but SPR510 appears to be the best candidate for the planarization process. It yields a smooth surface, controllable ash rate, and withstands the subsequent Mo and InGaAs etches. PMGI etches too rapidly, and BCB may be a strong candidate, but is much more cumbersome to work with than SPR510.

Future Work

The team must integrate the three distinct stages of the entire transistor fabrication process. The planarization process has been developed using gate stacks that mimic the samples that will be returned from the regrowth lab. The process must be fine-tuned from beginning to end with the gate stack fabrication, regrowth layers, and planarization process, as well as back-end processing.

Acknowledgements

A special thanks to the following people and organizations for their support: my principal investigator, Dr. Mark Rodwell; research mentor, Greg Burek; other team members, Uttam Singisetti and Dr. Mark Wistey; the UCSB cleanroom staff; the National Nanotechnology Infrastructure Network Research Experience for Undergraduates Program.

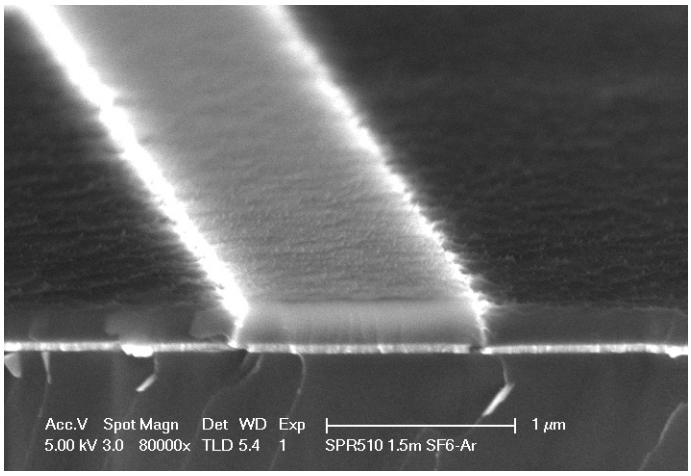

Figure 4: SPR510 after ICP and Mo etch.