Nanoscale Inhomogeneous Metal/Semiconductor Contacts

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Abstract:

Schottky contacts are commonly used in different high frequency, high temperature and high power electronic devices. Their electrical characteristics, and performance, critically depend on the nature of the metal/semiconductor interface. For a variety of reasons, diodes often contain small (typically 10 to 250 nm) patches of low-barrier height regions embedded in a background with a higher barrier height. Depending on the size and density of the patches, the diodes can exhibit significant non-ideality. In addition, determining the barrier height and density of the patches generally requires complementary materials characterization techniques coupled with modeling of the current-voltage characteristics. The goal of this project is to engineer inhomogeneous Schottky diodes by intentionally introducing low barrier regions to help us gain more insight into how to analyze the data from naturally-occurring inhomogeneous diodes. The size and density of these patches is controlled by the nanofabrication process, and we intend to correlate the observed electrical characteristics to the physical patch parameters.

Introduction:

Despite decades of intensive research about the formation of Schottky barriers (SBs) at metal-semiconductor interfaces (MS), they are still not fully understood [1]. Outstanding issues in the formation of SBs include the role of interface defect formation, electrode interdiffusion, and chemical reaction induced inhomogeneity at the interface of the metal and semiconductor [2]. The inhomogeneity is usually made up of low-barrier height regions embedded in a background with a higher barrier height. Depending on the size and density of the patches, the diodes can exhibit significant non-ideality. Therefore the goal of this research is to introduce low barrier regions with sizes ranging from 50 nm to 200 nm and various densities. The electrical characteristics will be compared with the physical characteristics to gain a better understand of naturally occurring inhomogeneous diodes.

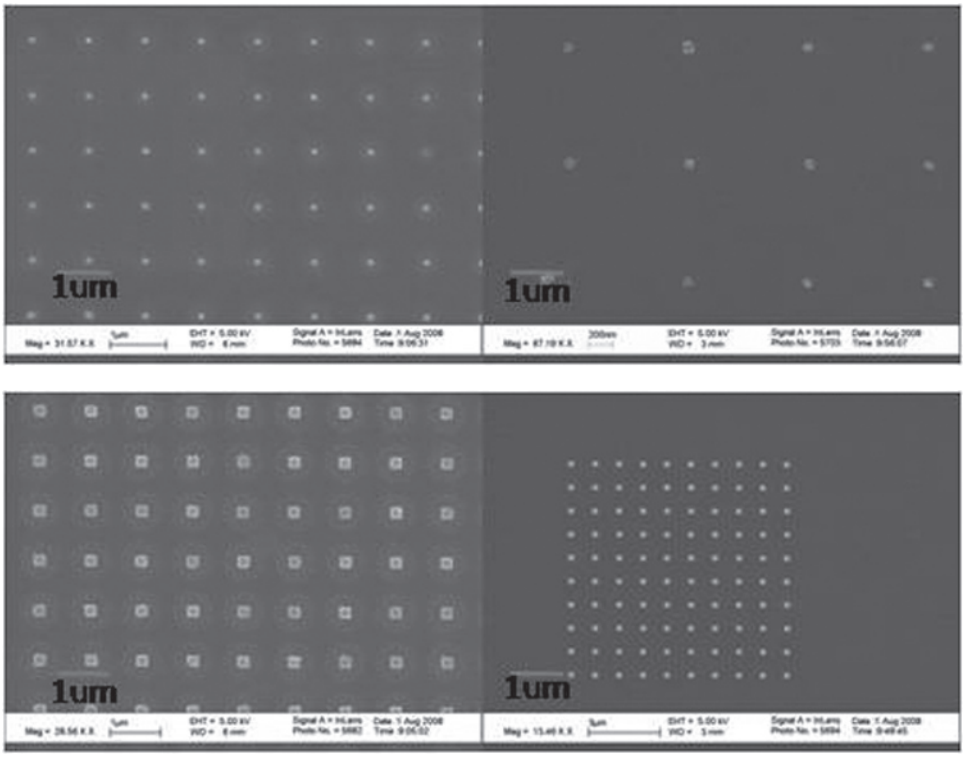

Figure 1, top: 50 nm dot before and after BOE etch.
Figure 2, bottom: 200 nm dots before and after BOE etch.

Experimental Procedure:

Our substrate was p-type silicon. 60 nm of aluminum was evaporated on the back of

our wafers. The samples were then annealed at 600°C for 30 seconds to form an ohmic back contact. ZEP520A resist was then spun on our samples at 4200 rpm for 45s to form a thickness of about 380 nm. Electron beam lithography was then performed to pattern the nanodots ranging from 50 nm to 200 nm, in three different areas. 95 nm of copper was evaporated at 2×10^{-7} torr in a vacuum for the low barrier metal. Liftoff was performed to define the low barrier regions. The samples were then etched in buffered oxide etch (BOE) which was made of 10:1 of ammonium fluoride and hydrofluoric acid for 10s to prepare the semiconductor surface for deposition of the higher barrier metal.

After the surface preparation, Shipley 1827 photoresist was spun on our samples at 4000 rpm for 45s. The samples went through the photolithography process. Alignment marks were utilized to pattern our 50 μm size high barrier regions on top of the nano dots. 65 nm titanium was then evaporated at 3×10^{-7} torr in a vacuum to form the high barrier metal. Liftoff was also performed to finish the inhomogeneous diode. Figures 1 and 2 are the 50 nm dots and the 200 nm dots before and after being etch in BOE for about 10s.

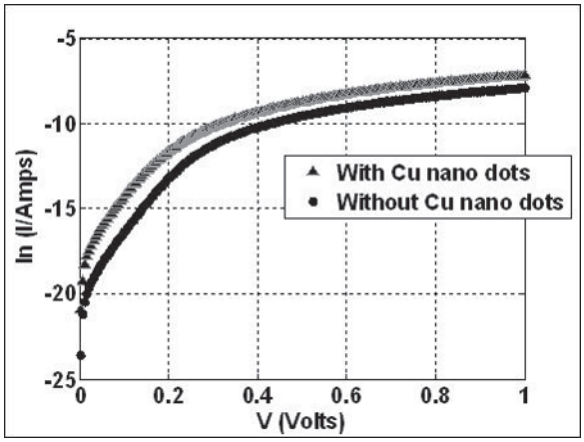

Figure 3: Plot of the homogenous and the inhomogeneous diodes.

Conclusions and Future Work:

Figure 3 is the plot of the homogenous and the inhomogeneous diodes. There was an upward shift in the current-voltage curve of the inhomogeneous diodes, which yielded a lower barrier height. The 0.1 increase of the ideality factor in the inhomogeneous diode may be due to the inhomogeneous nature of our diodes. Table 1 is the summary of our results. In the future, low temperature measurements will be performed to observe the double diodes' behavior of the inhomogeneous diodes.

M/S diode	Ideality factor (n)	Barrier height (eV)
Homogeneous	1.09	0.61
Inhomogeneous	1.19	0.57

Table 1: Ideality factor and barrier height extractions.

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References:

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