Graphene Nanoribbons as Transistors in Nanoelectronic Devices

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Abstract:

Graphene nanoribbons (GNRs) have recently been considered to be possible alternatives to silicon semiconductors in electronic devices. Graphene, a single layer of the carbon lattice structure graphite, has a high conductivity and electron mobility. When single sheets of graphene form narrow strips, they are considered GNRs. The properties of GNRs are being studied extensively because GNRs less than 10 nm wide have a band-gap suitable for making field-effect transistors (FETs).

In this project, the effects of the GNR dimensions on their electrical properties were analyzed. To make sure GNRs are suitable for use in nanoelectronic devices, the relationships between width and conductance as well as height and conductance must be understood. Our results indicated that, even at the nanometer scale, there is a positive relationship between both width and conductance and height and conductance.

Introduction:

As technology has advanced, the scientific community has strived to make electronics smaller and more efficient. These advances in technology and shrinking of electronic devices were largely due to the implementation of silicon semiconductors. However, there is a limit to how small one can design devices using silicon semiconductors, and that limit is being approached; the scientific community has begun to search for a suitable replacement. One option could be narrow graphene nanoribbons (GNRs). The high conductivity and ability to control the band-gap of GNRs by controlling their width makes GNRs an interesting option. For their successful implementation and the development of nanoelectronic devices using GNRs, their electrical properties must be studied and understood.

There are several different ways to produce GNRs. The process used for this project was that of "unzipping" multiwalled carbon nanotubes (MWNTs); the GNRs that are produced are high-quality, narrow, and have smooth edges.

The procedure for "unzipping" MWNTs has two steps: gas-phase oxidation and sonication. During gas-phase oxidation, the nanotubes were calcinated and small defects on the walls were etched away, producing a small hole. The nanotubes were then dispersed in a 1,2-dichloroethane (DCE) organic solution of poly(*m*-phenylenevinylene-co-2,5-dioctoxy-*p*-phenylenevinylene) (PmPV) by sonication, during which the carbon-carbon bonds were broken around the small hole and the nanotubes "unzipped" [1].

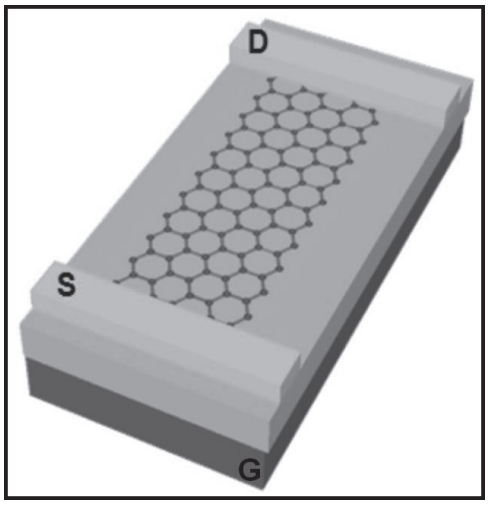

Figure 1: FET with source (S) and drain (D) Pd contacts, Si back gate (G), and SiO_2 dielectric.

The GNRs produced were suitable for making FETs. As seen in Figure 1, these FETs had source and drain palladium (Pd) contacts connected to the GNR, a Si back gate, and a 300 nm SiO2 dielectric [2]. Flow of current from the source to the drain was regulated by an electric field, produced by a voltage at the gate. The current produced by various gate voltages could be measured and the electrical properties of the individual GNR understood.

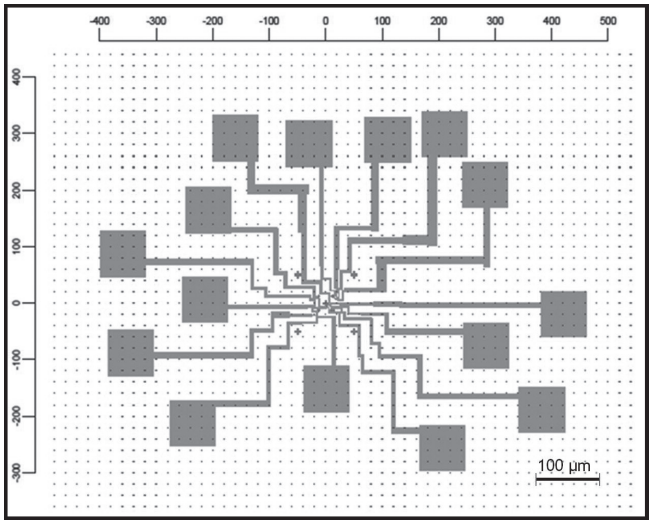

Figure 2: Final nanoelectronic device design.

Experimental Procedure:

Standard electron-beam-lithography (EBL) was used to expose markers onto a Si/SiO_2 wafer. The wafer was cut into small chips and a solution of "unzipped" GNRs was spin-coated onto the chips. Suitable GNRs were located on a chip using atomic force microscope (AFM); their widths and heights were also measured with AFM. The nanoribbons had to be straight, fully unzipped, and longer than one micron to allow for application of electrodes. Once several GNRs were located on a chip, the device was designed. Three to four 1 μm wide electrodes were placed across and perpendicular to the nanoribbon. As can be seen in Figure 2, the electrodes extended in a parallel and perpendicular sequence to an 80 μm wide contact.

Device fabrication consisted of four steps. First, EBL exposed the device pattern on the Si/SiO_2 chip. Second, Pd was deposited to coat the pattern and form Ohmic contacts with the GNRs. Excess Pd was lifted off of everything other than the device pattern. The final step was thermal annealing, which ensured that the Pd was in proper contact with the GNRs.

Testing of the device was achieved with a micro-probe station in vacuum at room temperature. The applied gate voltage was varied from -40 V to 40 V. If the electrodes were connected by a GNR, a current would flow through the device and a current (I_{sd}) vs. voltage (V_g) graph would be obtained. From this information, the electrical properties of each GNR could be studied.

Results and Conclusions:

Two relationships were studied during this experiment. The first was width vs. conductance. In Figure 3, it can be seen that there is a positive relationship between the width of GNRs of similar heights and the conductance. This information, compiled from GNRs of similar heights, shows that as width increases, conductance increases. Additionally, in Figure 4, there is a positive relationship of GNRs of similar widths and conductance. It is apparent that as height increases, conductance increases. Even at these small dimensions, these relationships hold.

With these values and the understanding of these relationships, the conductance of a GNR can be controlled when the dimensions of the GNR are controlled, producing specialized GNRs with specific properties that may be used in nanoelectronic devices.

Summary:

In this experiment, the electrical properties of GNRs were studied. These properties included the effect of width and height on conductance. Through the use of GNRs produced by "unzipping" MWNTs, simple FETs were fabricated. The procedure was a four step process of locating GNRs, designing devices, fabricating the devices, and testing the devices with micro-probe station.

The results indicate a positive relationship between both width and conductance and height and conductance of GNRs. Understanding these relationships is key to controlling the dimensions of GNRs and producing specialized GNRs for possible use in nanoelectronic devices.

Acknowledgements:

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References:

[1] L. Jiao. "Facile synthesis of high-quality GNRs." Nature Nanotechnology, 2010.

[2] L. Jiao. "Narrow GNRs from carbon nanotubes." Nature, 2009.

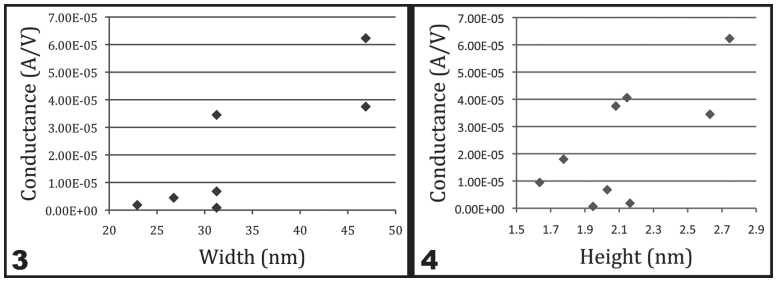

Figure 3: Width vs. Conductance graph of GNRs with similar heights.

Figure 4: Height vs. Conductance graph of GNRs with similar widths.