Rational Assembly of Semiconductor Nanowires via Dielectrophoresis

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MATERIALS

Abstract:

Rational assembly of "bottom-up" nanoscale structures such as nanowires has become a bottleneck limiting their real-world applications. Recent studies have achieved orientation control of the nanowires via directed assembly by fluidic flow or field-assisted techniques. However, these approaches still lack the control over location and end-to-end registry. In this project, we study rational assembly of nanowires with precise orientation and location control through dielectrophoresis (DEP). DEP assembly relies on the interaction of the induced dipole moment and an inhomogeneous electric field. As a result, the motion of a neutral subject, such as a nanowire, can be controlled by external voltages on nearby electrodes, leading to precise deposition of nanowires across the electrodes. The first part of this report discusses design and fabrication of the electrode patterns with features ranging from 0.5 μm to 7.0 μm, which enable the investigation of nanowire alignment with respect to feature size and nanowire length. In the second part, we report studies to explore the effects of external parameters such as voltage and frequency on DEP assembly. We report device yield over 80% via DEP.

Introduction:

As integrated circuits continue to aggressively scale down in size, novel nanostructures such as nanowires (NWs) have attracted increasing interest as essential components in future electronics. To date, the most widely used NW assembly techniques, such as directed assembly by fluidic flows [1], do not address the primary challenge of acquiring control of the position and registration of "bottom-up" grown NWs with the other components in a nano-scale device. DEP offers a potential solution to these problems and also holds the advantage of compatibility with established integrated circuit production [2]. In this project, DEP is used to precisely position NWs, utilizing the NW's high-aspect ratio and the tendency for matter to polarize in the presence of strong inhomogeneous electric fields and migrate to the region of highest field intensity [3]. By creating a photolithography-defined microscale electrode pattern that can produce an electric field that varies in a controlled manner across the sample, the effects of voltage, frequency, and electrode spacing on DEP can be studied and optimized.

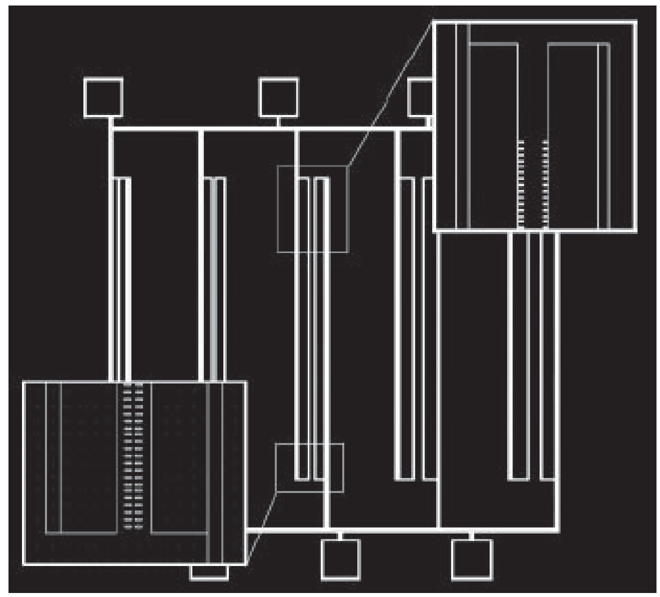

Figure 1: Reticle pattern for DEP testing.

Experimental Procedure:

A reticle that allows for simultaneous studying of multiple electrode spacings was created and designed with pairs of long, rectangular "bus" electrodes spaced 5, 15, 25, 40, and 50 μm apart, featuring evenly spaced pairs of "floating" electrodes of 1 x 4 μm in size and distanced 0.5 to 7.0 μm from the left and right bus electrodes (Figure 1). The floating leads design ensured parallel production of individually addressable nanowire devices. It also helped prevent burnout once a NW was bridged, as would normally occur from the heat generated by the AC signal during dielectrophoresis [4]. Silicon wafers with 500 nm of oxide were spin coated with LOR3A liftoff resist and SPR220-3.0 photoresist, exposed with a projection lithography system, developed with MIF300,

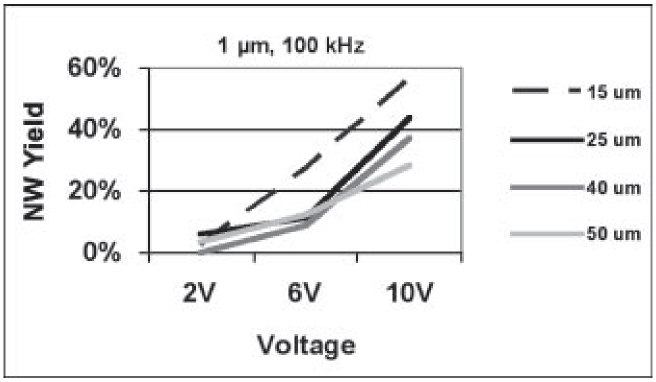

Figure 2: NW alignment yield for 1 µm finger-electrode spacing.

evaporated with 50 nm of Ti and 600 nm of Au, then placed in liftoff solution to remove excess metal.

DEP was then carried out to deposit NWs across the bus and floating leads. The applied voltage values ranged from 1.0-20.0 volts and frequencies were varied from 50 kHz to 1 MHz. In each DEP trial, a 0.5 μL drop of heavily-doped p+Si NW solution was dispensed onto the sample, and the AC signal was turned on for 50 s.

Results and Conclusions:

The effect of voltage on NW alignment was evident (Figure 2). As voltage was increased, more NWs were drawn towards the electrode pairs, and few NWs were observed outside the active device region because NWs had all migrated towards the regions of high field intensity (Figure 3). This was consistent with the expectation that higher voltages would create stronger electric fields, which in turn would draw in more NWs. NW alignment yields of up to 80% could be achieved. However, if the applied voltages were excessively high, it could render insignificant the field distorting effect of the floating fingers, causing NWs to densely align as though the floating leads were absent.

The device yield showed a non-monotonic dependence on frequency (Figure 4). The drop off of yield at very high frequencies was likely due to the inability of the nanowire polarization to follow up with the applied field. However, further studies including the dependence of frequency on DEP with respect to the finger-bus spacing will be needed to obtain a complete picture.

Future Work:

Further study of DEP would require research on various types of NWs and nanoparticles to explore other factors such as particle geometry and relative polarizabilities. It would also be possible to analyze effects of electrode patterning by designing floating leads with sharper ends mirrored by similarly sharp teeth on the surface of the electrodes. Such a design may further enhance the DEP effect and increase alignment precision.

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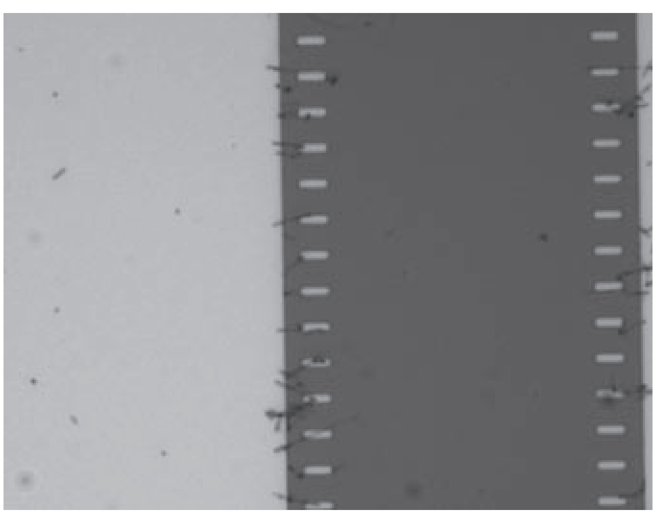

Figure 3: Optical image of NWs between fingers and electrodes.

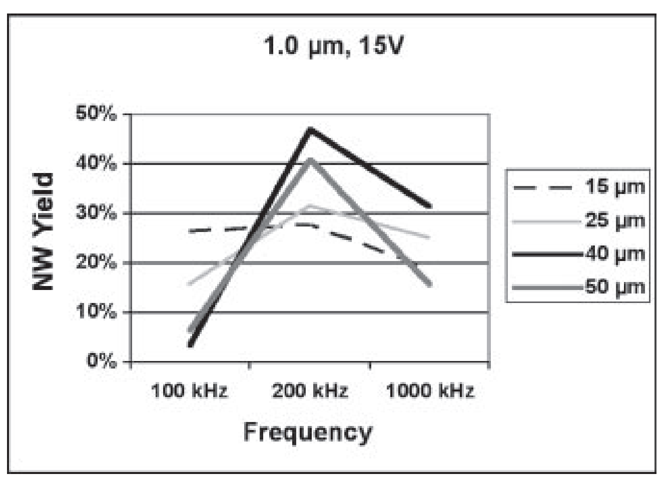

Figure 4: Effect of frequency on NW alignment yield.