Crystallization of Amorphous Silicon Nanowires using Electromigration and Self-Heating for TFT Applications

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Abstract:

Large area electronics, such as displays and touch screens, employ a network of thin film transistors (TFTs) to control image circuitry. The TFTs are commonly built on amorphous silicon (a-Si), providing small device-to-device variation, even though its mobility is much lower than other forms of silicon. Our goal was to investigate the possibility of crystallizing a-Si nanowires to form single crystalline areas by creating a single crystalline domain along a nanowire through self-heating and electro-migration techniques by application of electrical current. Employment of this technique in nanowires, rather than large area films makes it possible to achieve single crystal domains per wire rather than a polycrystalline structure, which would result in much higher carrier mobility while maintaining small device-to-device variations.

Introduction:

Displays require a high degree of uniformity in pixel arrangement to form desired images. This requires very small device-to-device variations in the device used for the driver circuitry and lighting element.

Thin film transistors, used in display technology, are fabricated from amorphous silicon (a-Si), due to uniformity of the material and overall cost, when compared with poly-Si and crystalline-Si fabrication. These two forms of silicon are not commercially used, but have greater electron mobility, as seen in Figure 1; making them superior candidates for future transistor fabrication.

Our solution to the problem of low mobility in a-Si was to use self heating and electro-migration to create a single crystal domain along a nanowire. Crystallizing a-Si reduces the interstitial boundaries between the atoms, decreasing electron collision and increasing mobility.

TFT Process	*Mobility (cm^2/V sec)*
A-Si	0.3-0.7
Conventional p	6
Eximer p-Si	329
Single Crystal Si (x-Si)	600

Figure 1: Mobility comparison among different silicon material.

When applying current to the nanowire, the internal temperature increases, allowing the embedded hydrogen to release and silicon atoms to re-arrange into a more orderly structure; beginning crystallization. Electro-migration is the bombardment of material atoms by electrons, causing detrimental erosion over time. By using this mobile force, we attempted to direct crystallization along the nanowire, resulting in a single crystalline domain. Preliminary experiments on making use of self-heating and electro-migration were investigated.

Experimental Procedure:

An array of nanowires connecting 100 μm x 100 μm contact pads were designed in a computer added design (CAD) program. The array ranged from 50 nm to 440 nm widths with 10 nm increments and lengths varying from 1.5 μm to 5.5 μm.

The nanowires were fabricated by depositing 200 nm of N-doped a-Si on a 776 nm silicon oxide, thermally grown on a silicon wafer. SPR-955 photo resist was spun at 4000 rpm for 60 seconds. Using the Auto Step (I-line optical stepper) and the designed mask, the wafer was exposed for 0.09 seconds resulting in nanowires that were 2x the size. The wafer was baked at 115°C for 90 seconds. Etching was performed in the Oxford 80; RIE using CF4 was the process used.

After fabrication, electrical current was passed through individual nanowires. An initial I-V measurement was taken to understand the preliminary electrical conductivity of the nanowire. A constant voltage was then applied to the wire, ranging in bias and time duration based on wire dimensions. This voltage application was repeated many times, to determine what effect current had on the nanowire. A final I-V measurement was taken for electrical comparison. Electrical testing was completed when the wire was either deemed broken or near the breaking threshold.

Results and Conclusion:

After electrical current had been passed, a noticeable discoloration was first observed. The nanowire and electrode pad changed from a blue hue to a pink tint; the nanowire being most vibrant. The electrode pad measuring incoming voltage remained unchanged. Discoloration of the a-Si is probably due to the occurrence of oxidation.

We examined the nanowires using a scanning electron

microscope (SEM) to verify whether the nanowires were broken or intact. Cracking was observed to extend into the pad areas, shown in Figure 2, which suggested significant electromigration or internal mechanical stress. Another observation was the formation of white bubbles along the side of the nanowire, which could not be explained. Some texture change was observed in the nanowires around the crack regions, but no crystallization was seen.

In order to increase flexibility within the nanowires, silicon oxide was etched beneath the N-doped a-Si using buffered oxide etch (BOE) solution, removing 500 nm of silicon oxide. This etching resulted in suspended beams. Electrical testing was performed again on various nanowires.

Results of the testing provided interesting findings. The first nanowire to show significant crystallization was a 250 nm BOE nanowire. An SEM image of the nanowire, seen in Figure 3, showed considerable grain alteration on the side closest to the applied voltage. The crystallization is visible by color dissociation. Crystallization did not progress along the entire length of the nanowire, but instead stopped where the nanowire broke, due to material disparities.

Complete crystallization along the whole length of the nanowire can be seen in Figure 4. The nanowire broke when 30 μV was applied over a fraction of a second. This was a mishap that occurred due to forgetting to reset the voltage from a previous test. The excessive voltage increased the temperature above 1414°C, high enough to melt the a-Si; and cooled rapidly when the current flow stopped. The nanowire solidified into a smooth rounded structure, tapering to the breakage point. The smoothen nanowire is distinguished from the surrounding non-crystalline material due to a change in surface granulation. This nanowire is the best candidate for single grain crystallization and TEM imaging of the atomic structure would provide verification.

The experiments on these nanowires are presently used to investigate the time scales and the necessary voltage which should be applied to form crystalline nanowires while keeping the wires attached the contact pads.

Acknowledgements:

I would like to thank my PI and mentor Ali Gokirmak for his strong dedication and influence in helping me to learn. Many thanks to my research site at Cornell University, and Melanie-Claire Mallison for making sure the wheels of success ran squeaky free. Thanks to National Nanotechnology Infrastructure Network for funding this great research opportunity of which I was most appreciative to be a part.

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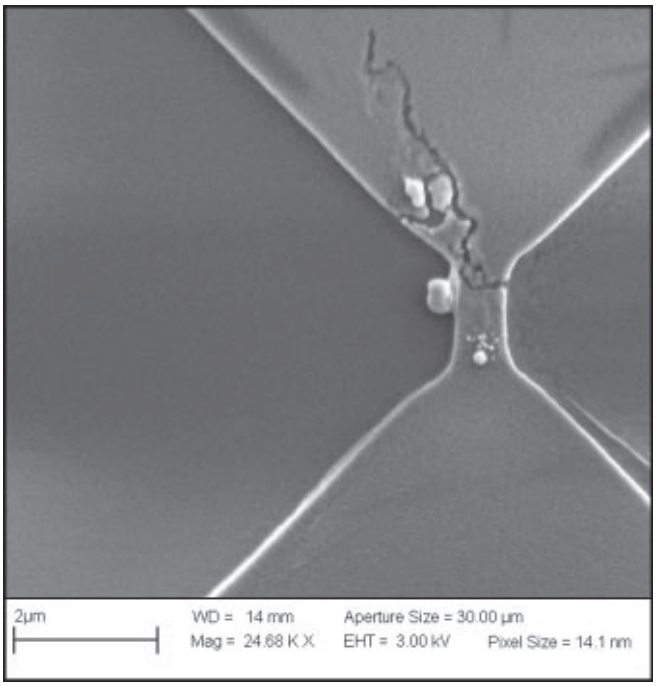

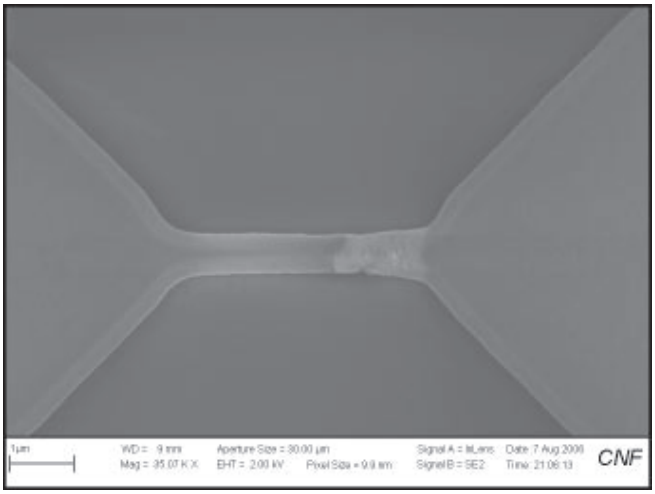

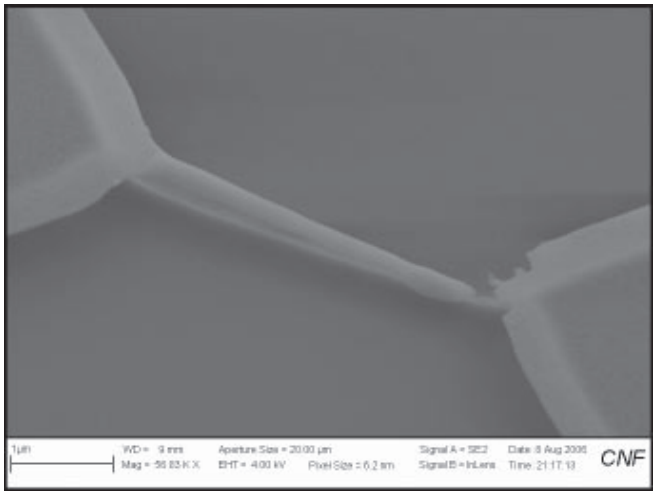

Figure 2, top: SEM image of 200 nm RIE etched nanowire.

Figure 3, middle: SEM image of 250 nm BOE nanowire.

Figure 4, bottom: SEM of 140 nm crystallization of nanowire.