



Dry Etch of III-V, and Si Materials at UCSB

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Adapted from Hwang and Giapis, JVST B15, 70, (1997)

















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InP-Based Etch





Unaxis VLR tool

- Chlorine-based Load-locked System, turbo-pumped
- *RT* 200 *C*, 4" Electrode, Heated walls and liner, ceramic clamp
- He cooling. Pieces mounted with DOW silicone thermal grease
- 1 kW, 2 MHz ICP source, 500 W RF Bias source
- Laser monitoring Vis.
- Cl₂, BCl₃, H₂, O₂, Ar, SF₆, N₂
- InP and related compounds, all other III-V As,N,P,Sb materials

Primarily used for InP and related compounds at 200 C etching temperature, due to $InCl_X$ volatility issues

SF6 added to chamber for selective etching of GaN/ AlGaN

Sapphire and Silicon carrier wafers used.







Hydrogen was introduced into the chamber to create H⁺ ions in plasma to neutralize the excess electrons on side-wall



InP Etch with Cl₂/H₂/Ar Chemistry Flat Trench Bottom (no Micro-trench)



Unaxis VLR: 1.5mT, 125/800W, Cl₂/H₂/Ar Flow-rate=7.4/11.6/2SCCM, and time=90 s Etch Rate=1.57µm/min (open area), Etch Selectivity(InP/SiO₂)=15.5 (N. Cao)



InP Etch with Cl₂/N₂/Ar Chemistry Micro-trench at Trench Bottom



Unaxis VLR: 1.4mT, 125/800W, $Cl_2/N_2/Ar$ Flow-rate=7.4/11.6/2SCCM, and time=120 s Etch Rate=0.69 μ m/min, Etch Selectivity(InP/SiO₂)=9.3 (N. Cao)





InGaAs nano-wires: 1.5mT, 125/800W, $CI_2/H_2/Ar=7.4/11.6/2SCCM$, and time=60 s (Fig. a: SiO₂ etch mask)





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GaN- and GaAs-Based Etching



RIE #5



Plamsa Therm 770 SLR system

- 500 W Power supply.
- Stainless Steel Housing. No liner. Ceramic clamp (Alumina)
- RT 80 C, 4" electrodes with clamp and He cooling
- Variable Upper Electrode Height
- HeNe Laser monitoring
- *Cl*₂, *BCl*₃, *SiCl*₄, *O*₂, *Ar*, *N*₂
- AlGaAs, AlGaN, Ti, Al, Si, Other materials
- Masks: PR, SiNx, SiO2, SrF2, Ni

Oxygen cleans often used before runs to clean chamber System needs wet clean ~ every 2 months. Cleaned at first signs of arcing System is down for 3 days minimum after wet clean









- Performed a pretreatment etch in BCl₃ to remove surface oxides
- Etched facets using two-layer PR as an etch mask → results in a smoother facet etch
- Verticality of PR mask controlled by optimizing exposure time
- Etch conditions (Plasmatherm RIE #5):
 - Pressure: 5 mTorr
 - Cl₂ flow rate: 10 sccm
 - *RF power: 200 W*





Bi-Layer Resist Mask













Etched Facet Cross Section



























GaAs/AIGaAs Post Etch: 5mT, 110W, SiCl₄=10sccm, Etch rate: ~90 nm/min. PR mask (still remaining on the top) B. Thibeault







Silicon Deep RIE/ICP – Bosch



Si- DRIE



Plasma-Therm 770 SLR

- Fluorine-Based Bosch Process (Cyclic etch/dep process)
- 1kW, 2 MHz ICP source, 4" wafers, 500 W Sample Bias
- Pieces mounted with Diff Pump Oil: Santovac 5 (Polyphenyl Ether) or thermal tape
- He cooling, ceramic clamp
- Si-deep etching for MEMS
- > 3um/min etch rates possible
- SF₆, C₄ F₈, O₂, Ar, N₂
- PR, SiN, SiO₂, AIN masks
 Selectivity up to 300:1 with oxide
 Up to 80:1 with PR

20 minute Bosch Season run done before etch if system idle for more than 30 minutes. Wet cleans done on as-needed basis.

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UCSBOne-step Si etch (remove "scalloped" sidewall profile of Bosch process)





*C*₄*F*₈/S*F*₆/Ar: 50/30/20SCCM

*C*₄*F*₈/S*F*₆/Ar: 52/28/20SCCM

 $C_4F_8/SF_6/Ar: 54/26/20SCCM$

Etch Conditions: total gas flow=100SCCM, 19mT, 9/850W copied from Yung-Jr Hung, et al.'s paper







One-step Si etch (narrow trench etching)





a, b: SiO₂ etch mask pattern



c,d: After one-step Si etch. Etch condition: 19mT, 15/825W, $C_4F_8/SF_6/Ar$: 54/26/20 SCCM, and time=3min, Etch rate: 171 nm/min (N. Cao)





One-step Si etch (nanowire etching)





a, b: SiO₂ etch mask pattern



c,d: After one-step Si etch. Etch condition: 19mT, 15/825W, $C_4F_8/SF_6/Ar$: 54/26/20 SCCM, and time=5min, Etch rate: 200nm/min (N. Cao)





One-step amorphous Si etch, 19mT, 15/825W, $C_4F_8/SF_6/Ar$ flow-rate=54/26/20 sccm









Application: Thermoelectric Devices with Etched Si Nano-wire Array





Fig. 1. The vertical Si NW composite thin-film device structure used in this work, illustrating the top contact, Si NWs embedded in a matrix material, and Si substrate bottom contact.

Fig. 2. Scanning electron microscope images of Si NW/SOG substrate fabrication after:(c) etching Si to form Si NWs (SiO2 mask not removed), and (d) embedding the Si NWs with SOG and curing the composite film.





Copied from B.M. Curtin et al.'s paper: J. Elec. Mat., V41, pp887-894, 2012





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Si Etch with XeF₂



