Georgia Institute of Technology
Plasma Etch Equipment

Process Engineer: Hang Chen

Equipment Engineer: Thomas Johnson-Averette

Credit to Brittany Opraseuth
for creating this presentation

Institute for Electronics and Nanotechnology

Cleanroom website:
http://cleanroom.ien.gatech.edu

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Etch Equipment Overview

- STS Multiplex ASE DRIE
- STS Multiplex DRIE AOE
- STS Multiplex DRIE SOE
- STS DRIE ASE Pegasus
- PlasmaTherm Dual DRIE SLR
- PlasmaTherm SLR RIE
- PlasmaTherm RIE
- Advanced Vacuum Vision RIE 1
- Advanced Vacuum Vision RIE 2
- Unaxis RIE*
- Oxford Cryogenic ICP*
- Oxford Endpoint-RIE*
- STS HRM*
- Y.E.S. R1 Plasma Cleaner*
- Gasonics Asher 1
- Gasonics Asher 2*
- Xactix Xenon Difluoride e1 Series Xetch

* : denotes recent acquisition

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STS Multiplex ASE DRIE

Pettit Cleanroom

Advanced Silicon Etcher

Function:

- Deep Silicon Trench Etching (Bosch process)
- SOI Wafer Etching

Materials etched and acceptable masks:

- Etched: Si, poly-Si, a-Si
- Masks: Photoresist, SiO_2, Si_3N_4
- No SU-8, BCB, metal

Component Specifications:

- 1000W 13.56MHz ENI ACG_10B – Coil
- 500W 13.56MHz ENI Platen
- 300W 380kHz AE LF-5
- Backside Helium Cooling with Standard 8-pin ceramic clamp & lip seal

Gases: C_4F_8, SF_6, O_2, Ar

Substrate size: small pieces – one 100mm wafer

Process pressure: 2-80mT

Temperatures:

- Platen 5°C to 40°C, Walls 40°C, Lid 45°C

Vendor-specified Capabilities:

- 30:1 Aspect Ratio 1µm trench
- 15:1 Aspect Ratio 1µm on SOI with minimal notching

Actual:

- 43:1 Aspect Ratio 1µm trench gratings

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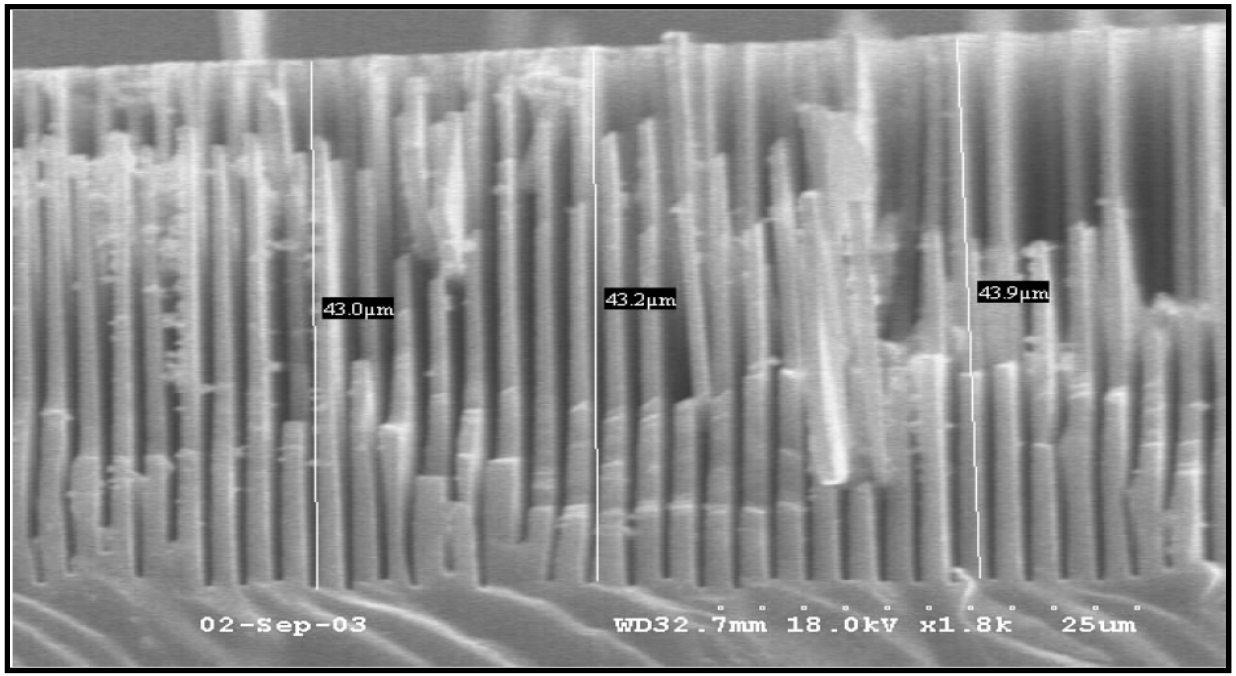
STS DRIE ASE best results: 43:1 AR on 1µm trenches

Image provided by Eric Woods, P.I. James Zhou, MiRC

- SiO_2 mask
- High gas flow rates
- Higher etch to passivation step times ratios
- Lower platen power



*Damage shown to trench sidewalls caused by cleaving process. Fins were prone to breakage, so trenches were partially filled with SiO_2, cleaved, then released using HF and a supercritical CO_2 drying process.

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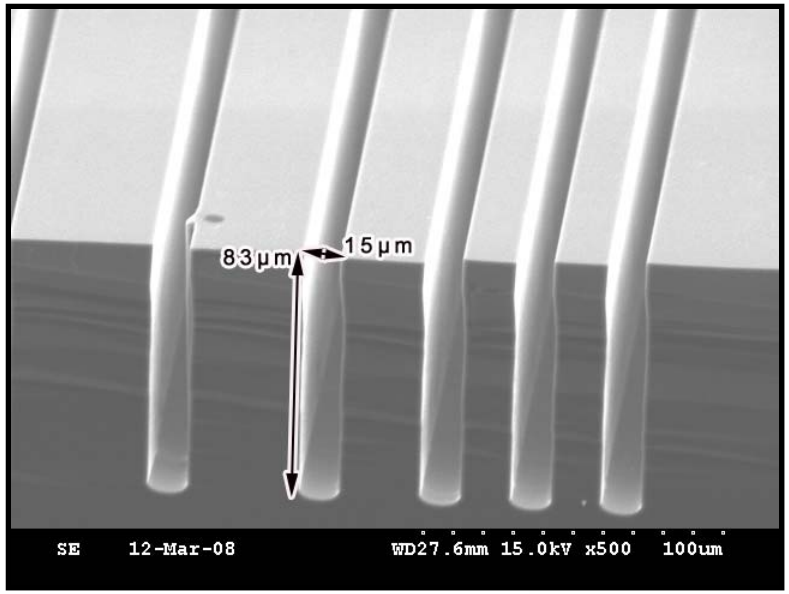
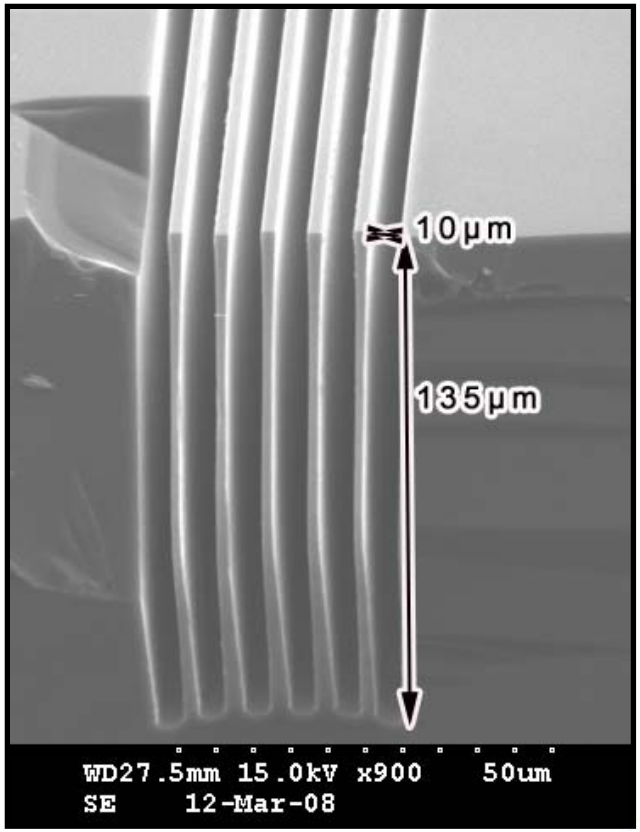
STS DRIE ASE examples

Images provided by Eric Woods and Erin Walters, MiRC





Rules:

- Silicon etching only
- No exposed metal
- CMOS compatible processes only
- No through-wafer etching without carrier wafer
- Backside of wafer must be clean

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STS Multiplex DRIE AOE

Pettit Cleanroom

Advanced Oxide Etcher

Functions:

- High aspect ratio etching with high etch rate and selectivity

Materials etched and acceptable masks:

- Etched: SiO_2, quartz, Pyrex, fused silica, Si_3N_4, bulk silicon
- Masks: Si, PR & Metals (Cr, Ti, Ni)

Component specifications:

- 3000W 13.56MHz AE – Coil
- 1000W 13.56MHz ENI – Platen
- Backside Helium Cooling with Standard 8-pin clamp & lip seal

Gases: C_4F_8, SF_6, O_2, H_2, CF_4, two open gas slots

Process Pressure: 2-80mT

Substrate size: small pieces - one 150mm wafer

Temperatures: Platen -20°C to 120°C, Walls 100°C, Lid 120°C

Vendor Specified Capabilities:

- 2.5µm isolated trenches on 8-10µm TEOS
- Etch rate >2000Å/min SiO_2, >4:1 selectivity SiO_2: PR, etch rate variability intra- and inter-wafer ±3%, sidewalls 85-90°

Actual capabilities when tool acquired

- 5µm features on 3-10µm SiO_2
- Etch rate >3000Å/min SiO_2, >7.5:1 selectivity SiO_2:PR, etch rate variability intra- and inter-wafer ±2%, sidewalls 89-90°

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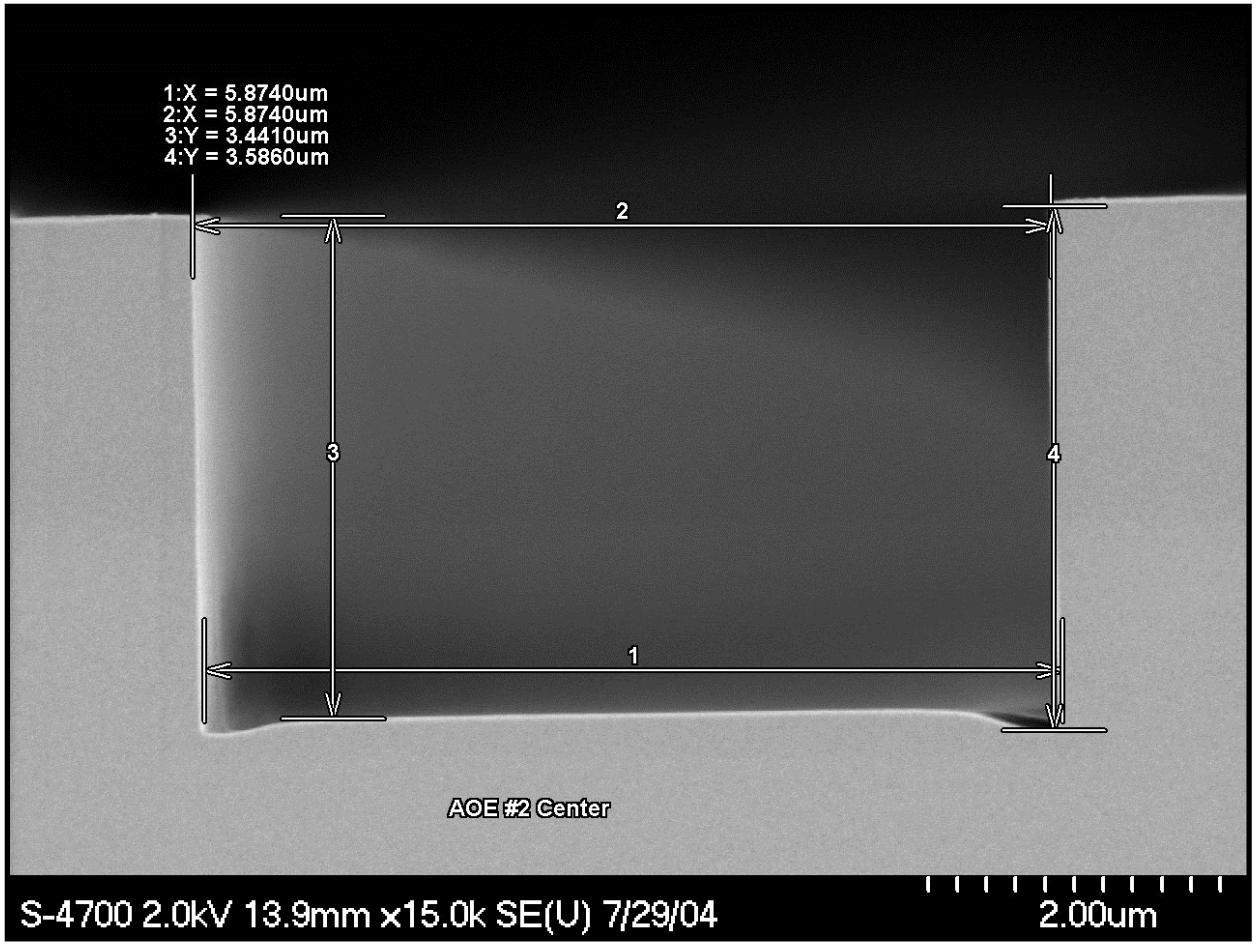
STS DRIE AOE examples

Images provided by Greg Kally, Mary Winters, and Judy Sline, Infotonics and Jeff Hawks, STS



Images from AOE process qualification August 2, 2004

Gases: C_4F_8, H_2

Pressure: 4mTorr

Temp: -10°C

Small microtrench formation at bottom of trench

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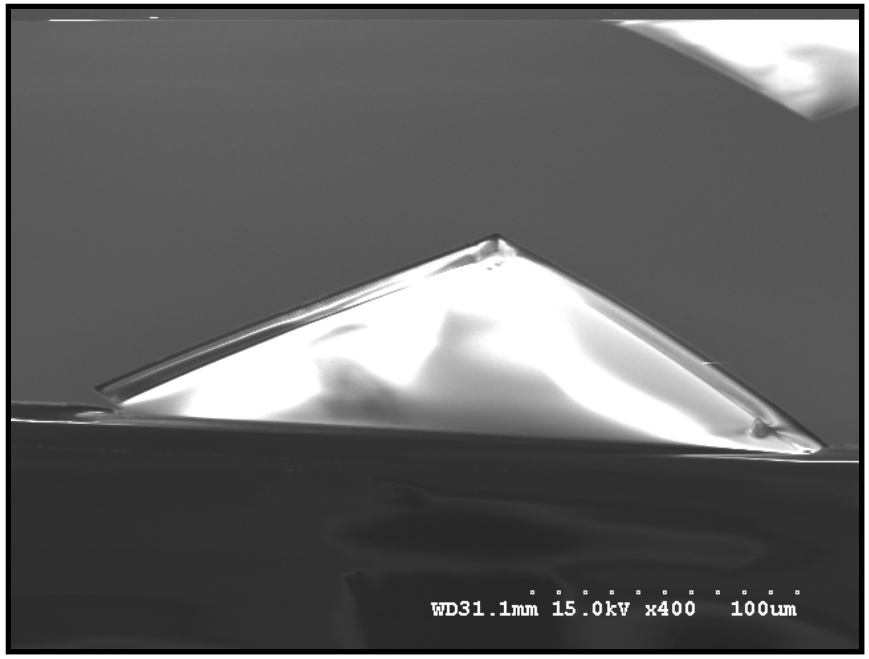
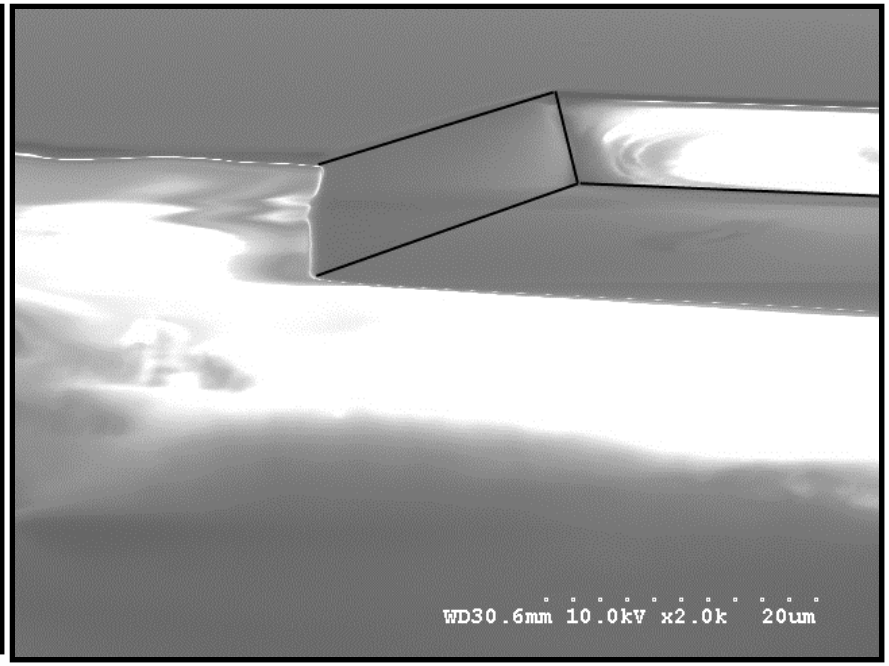
STS DRIE AOE: chrome mask

Images provided by Xin Gao. PI: Farrokh Ayazi, GT ECE





Chrome etch rate	323Å/min
Pyrex etch rate	0.282µm/min
Selectivity	25.6 : 1

Sample: Etched Pyrex with Cr removed

Feature size: 150µm

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STS DRIE SOE

Pettit Cleanroom

Standard Oxide Etcher

Functions:

- Shallow silicon trench etching
- III-V etching

Materials etched and acceptable masks:

- Etched: SiO_2, Si (<10µm)
- Etched: III-V → InP, GaN, InAlGaAs
- Masks: Si_3N_4, SiO_2, III-V, photoresist

Component specifications:

- 1000W 13.56MHz ENI – Coil
- 300W 13.56MHz ENI – Platen
- Backside Helium Cooling with Standard 8-pin clamp & lip seal

Gases:

- CH_4, H_2, Cl_2, BCl_3, HBr, CHF_3, CF_4, Ar, O_2, N_2 one open channel

Process Pressure: 2-80mT

Substrate: small pieces - one 100mm wafer

Temperatures:

- Platen -20°C to 180°C, Walls 40°C, Lid 45°C

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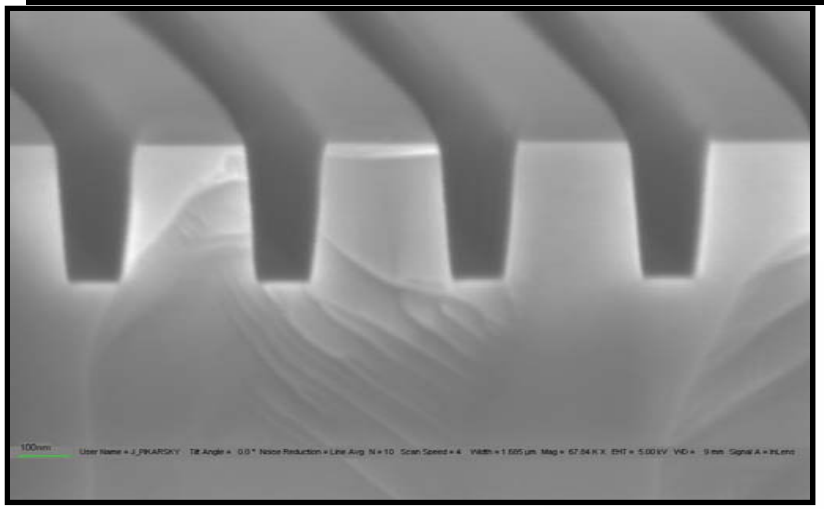
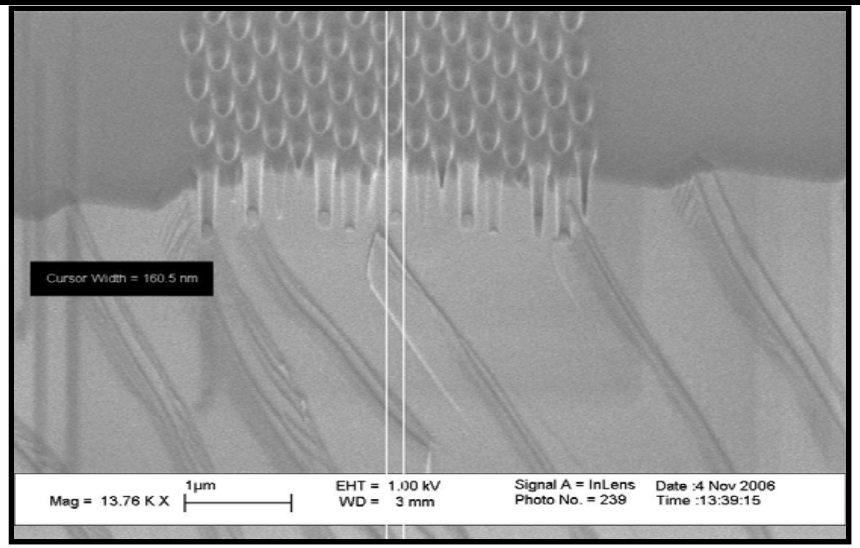
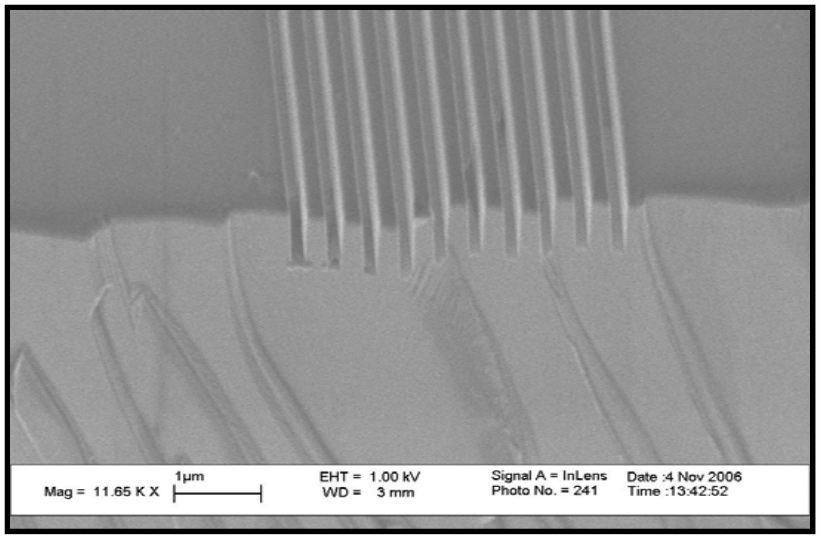
STS DRIE SOE: GaN

Images provided by Ehsan Hosseini. PI: Ali Adibi







- Gases: Cl_2
- Mask: SiO_2
- Grating Structure

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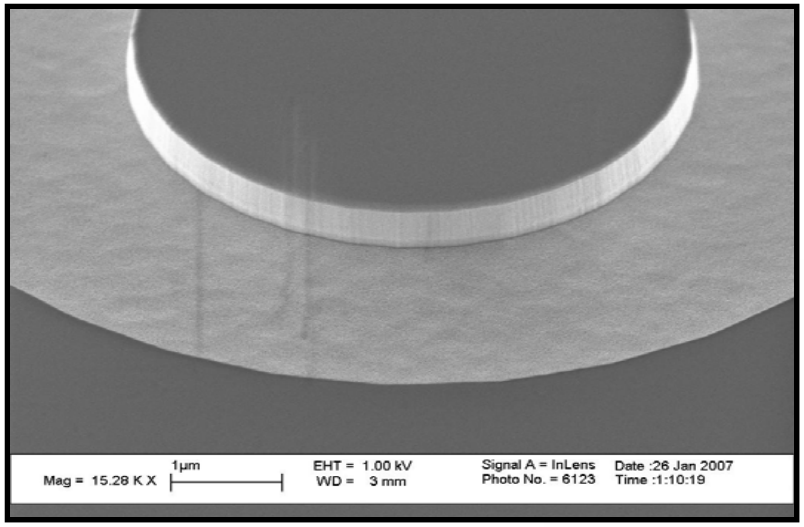
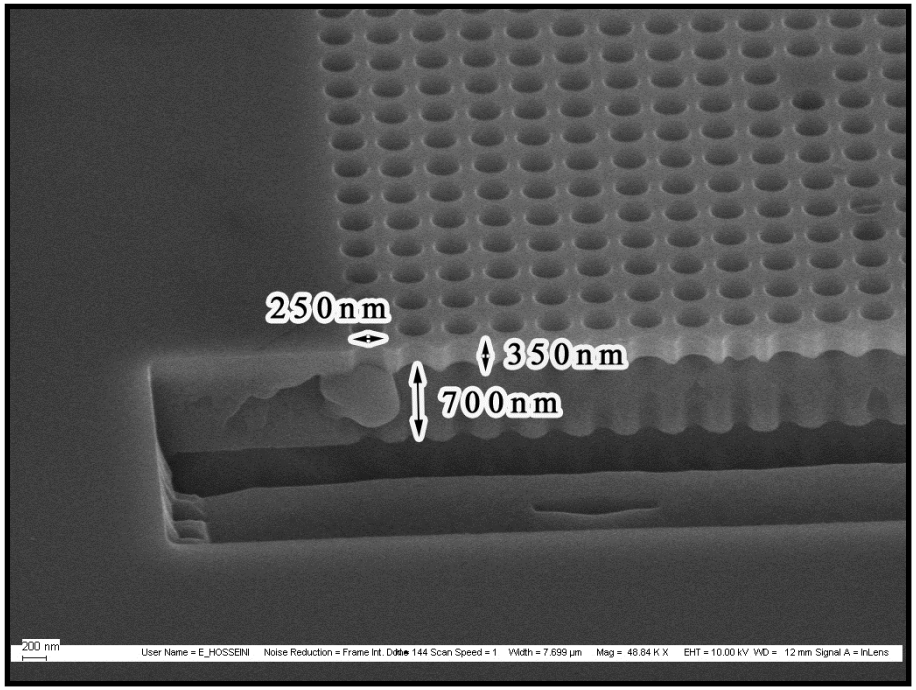
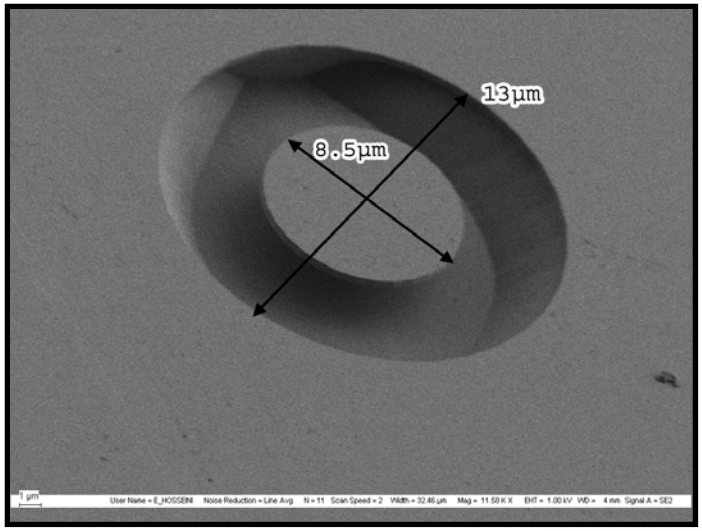
STS DRIE SOE: InAlGaAs

Images provided by Ehsan Hosseini. PI: Ali Adibi







- Gases: BCl_3, CH_4, Ar
- Mask: SiO_2 / Si_3N_4
- Photonic Crystal

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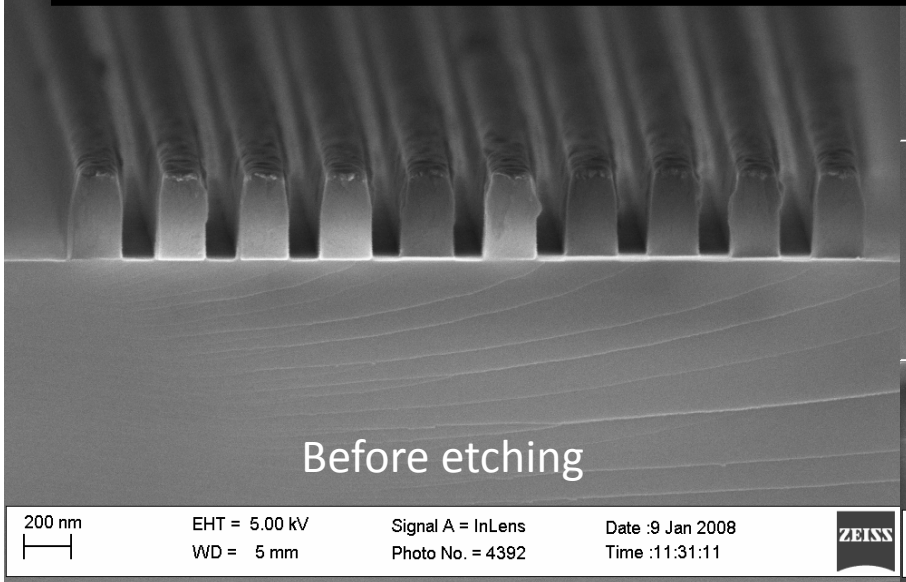
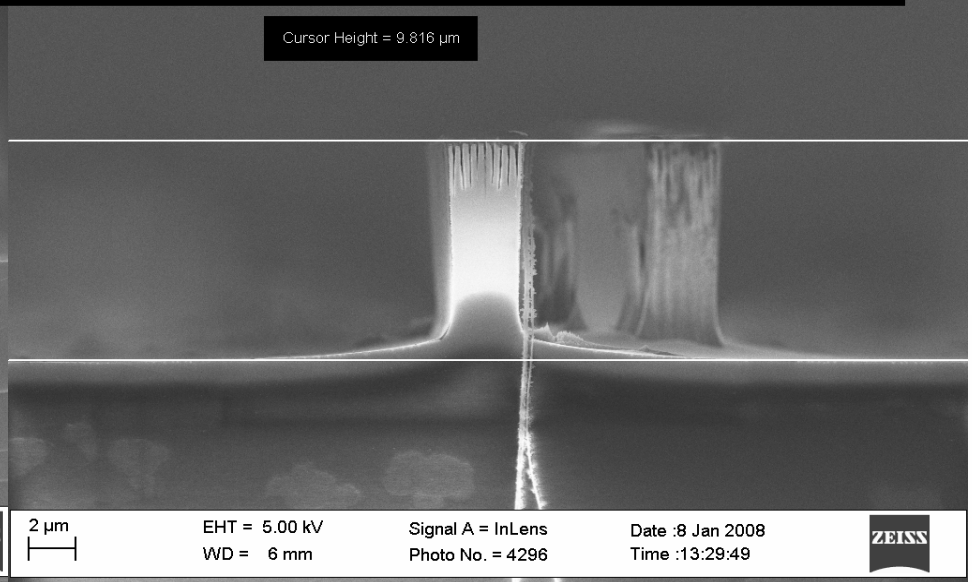
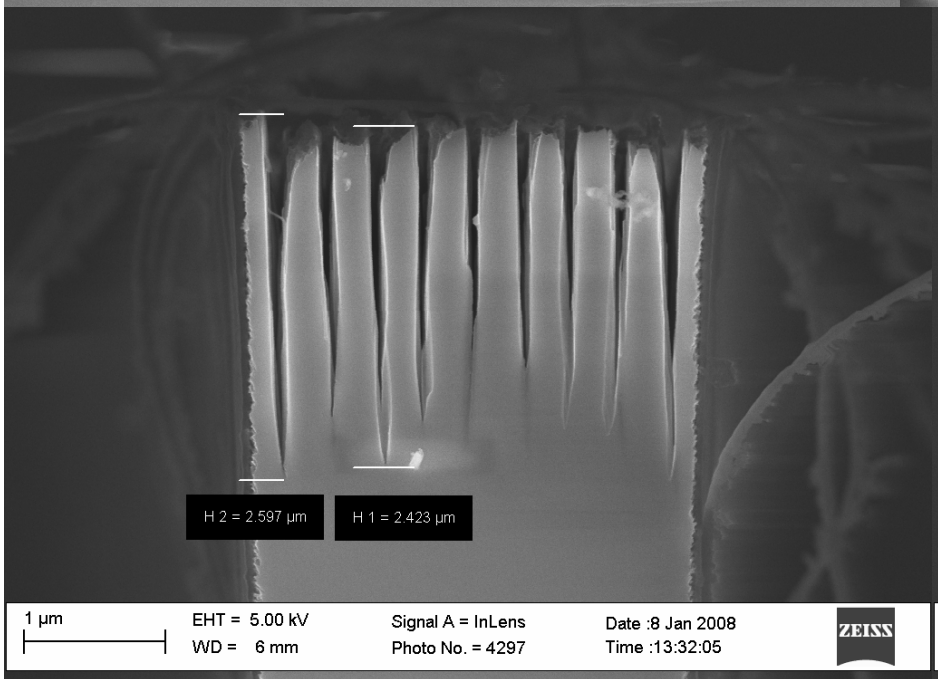
STS SOE DRIE, EBL5-SOE-3 – Dec 2007 – InP

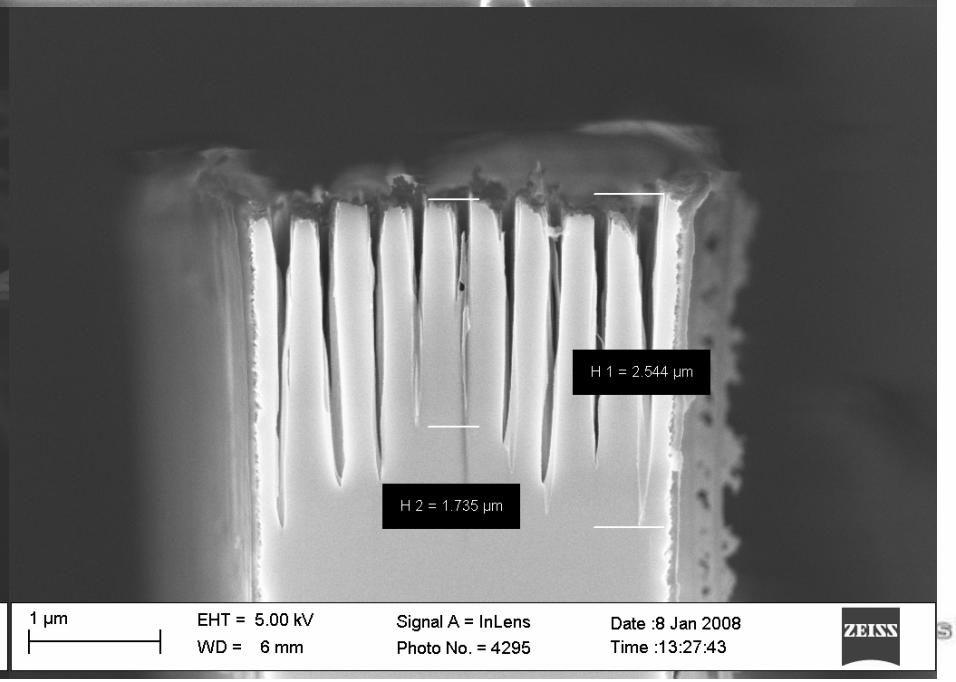
Time: 3min, Press: 4mT,, Gases: HBr & BCl3

Images provided by Ehsan Hosseini. PI: Ali Adibi.



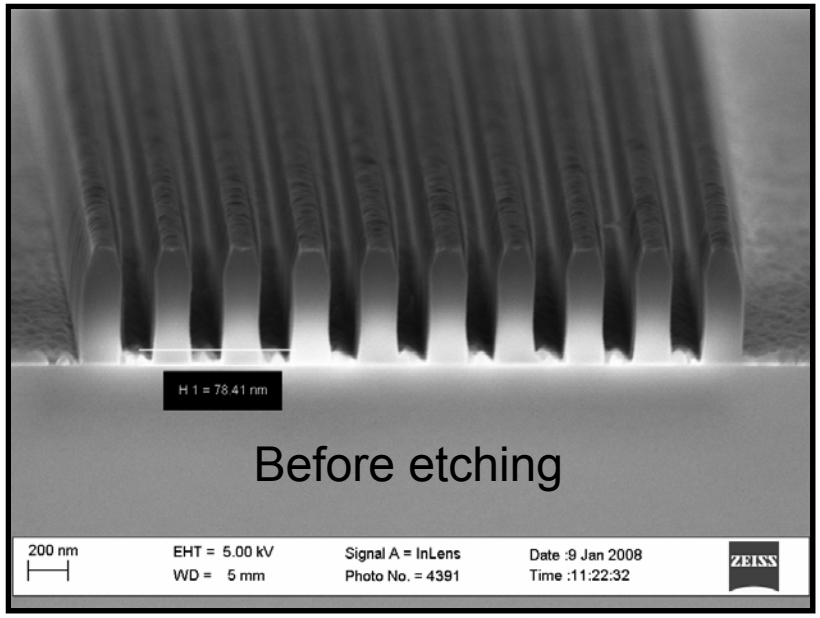


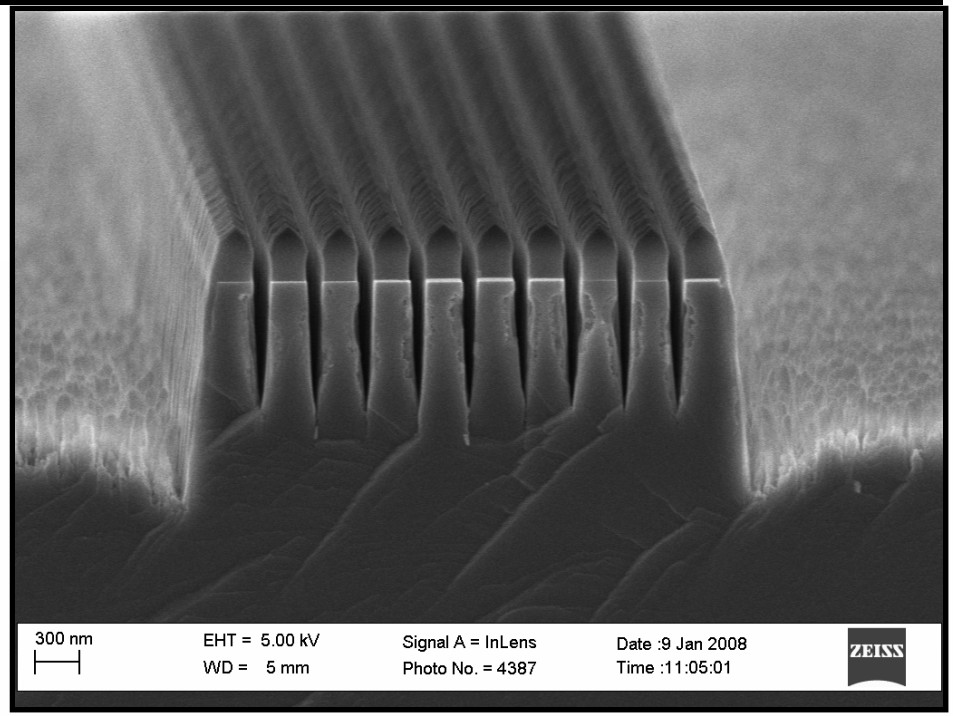




STS DRIE SOE: InP, Dec 2007

Images provided by Ehsan Hosseini. PI: Ali Adibi





Sample: InP with SiO_2 mask
Feature size: 200nm line width
Mask thickness: 600nm (before), 400-450nm (after)
Etch depth: 1000nm

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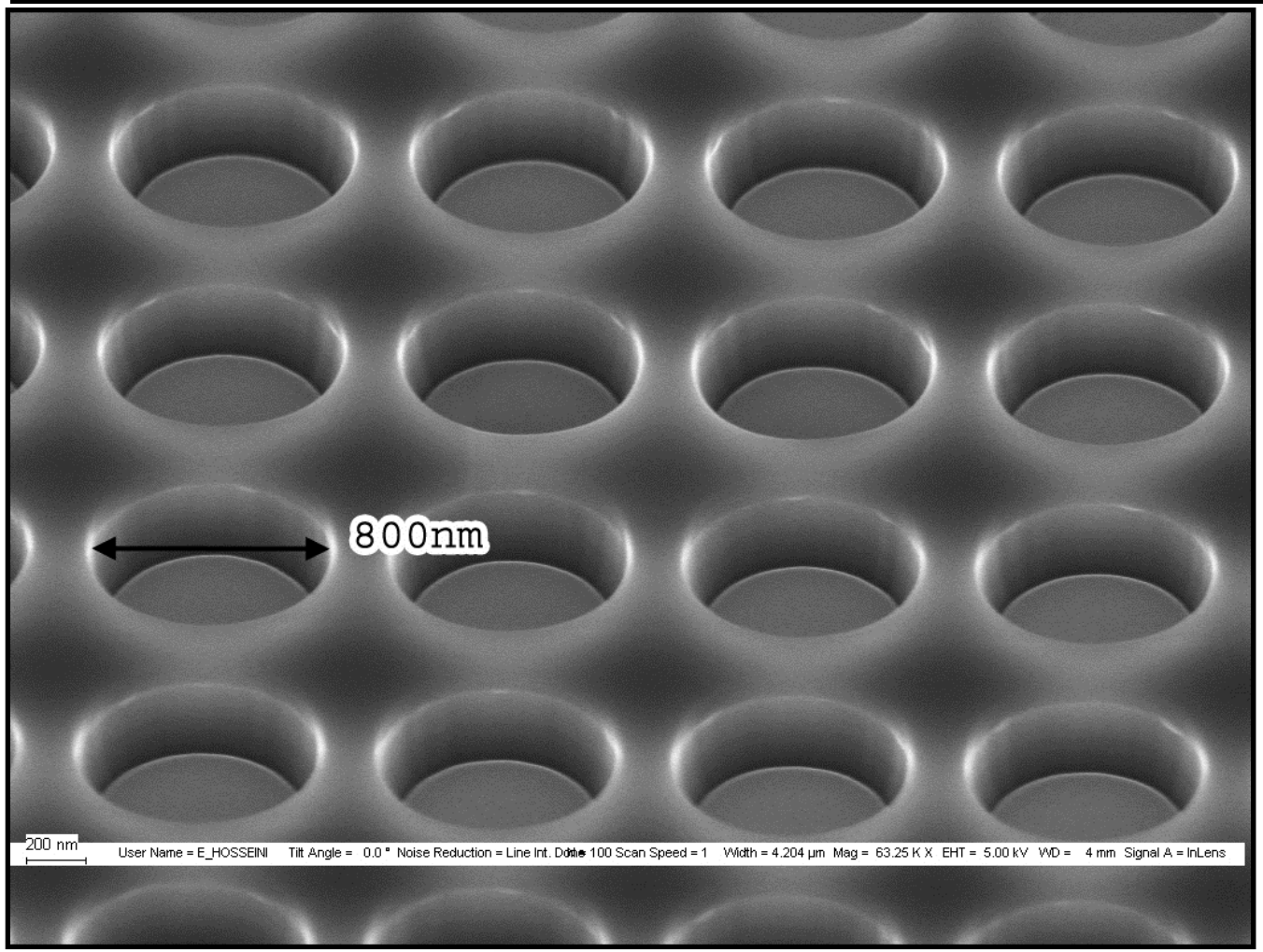
STS ICP SOE: Silicon

Images provided by Ehsan Hosseini. PI: Ali Adibi



Gases:

Cl_2, HBr, Ar

Feature Size:

- 800nm width
- 500nm depths

Mask:

ZEP resist

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STS ICP ASE Pegasus

Pettit Cleanroom

Tool Currently Installed / STS Qualifying Processes

Function:

- Silicon Trench Etching (Bosch process)
- First Pegasus installed in US university

Materials etched and acceptable masks:

- Etched: Si, poly-Si, α-Si
- Masks: Photoresist, Si_3N_4, SiO_2

Component Specifications:

- 5000W 13.56MHz MKS – Coil
- 500W 13.56MHz ENI -- Platen
- 300W 380kHz AE LF-5
- Backside helium cooling with electrostatic chuck

Gases: C_4F_8, SF_6, O_2, Ar

Substrate size: small pieces – one 100mm wafer or 150mm capability

Process Pressure: 2-80mT

Temperatures:

- Platen -20°C to 40°C, Walls 120°C, Lid 120°C

Vendor Specified Capabilities with 10% exposed Si (Width : Trench Depth):

- 0.5µm : 30µm SOI (LF platen)
- 0.2µm : 10µm SOI (LF platen)
- 3µm : 100µm (HF platen)
- 2µm : 60µm (HF platen)

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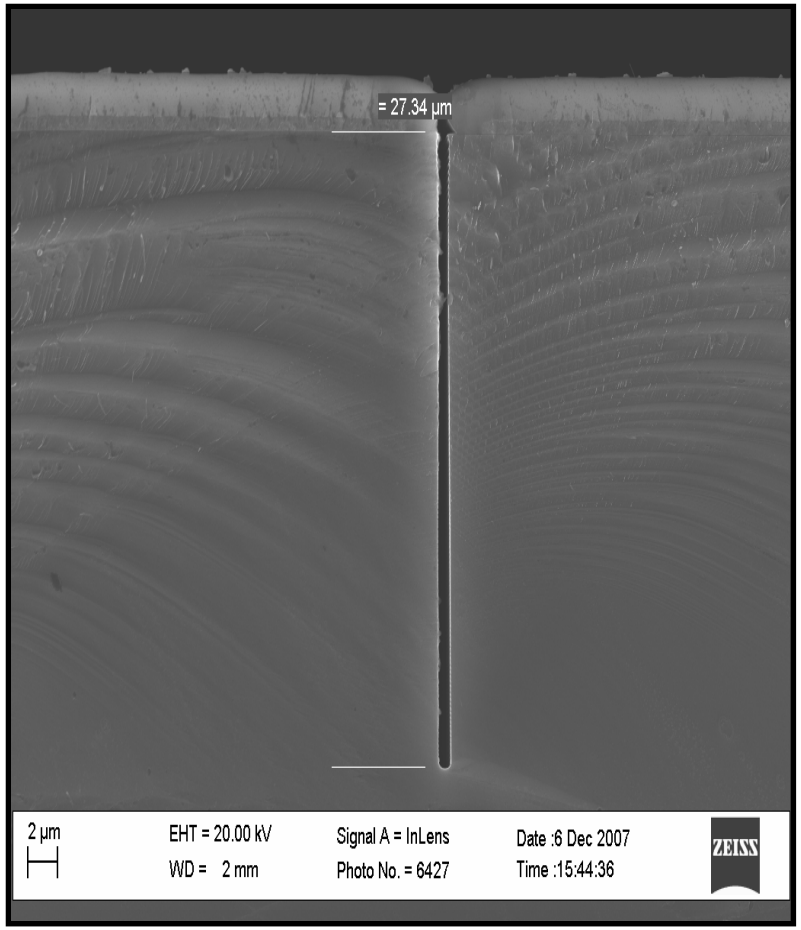
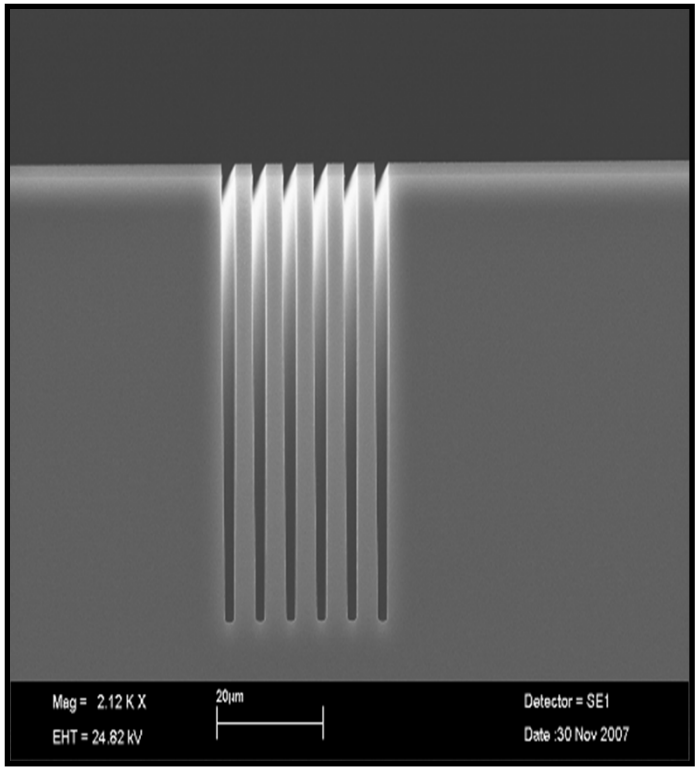
STS DRIE ASE Pegasus tool

Images provided by Varun Keesara & Prof. Farrokh Ayazi



Width:Trench Depth
0.5µm:27µm



Width:Trench Depth
2µm:60µm

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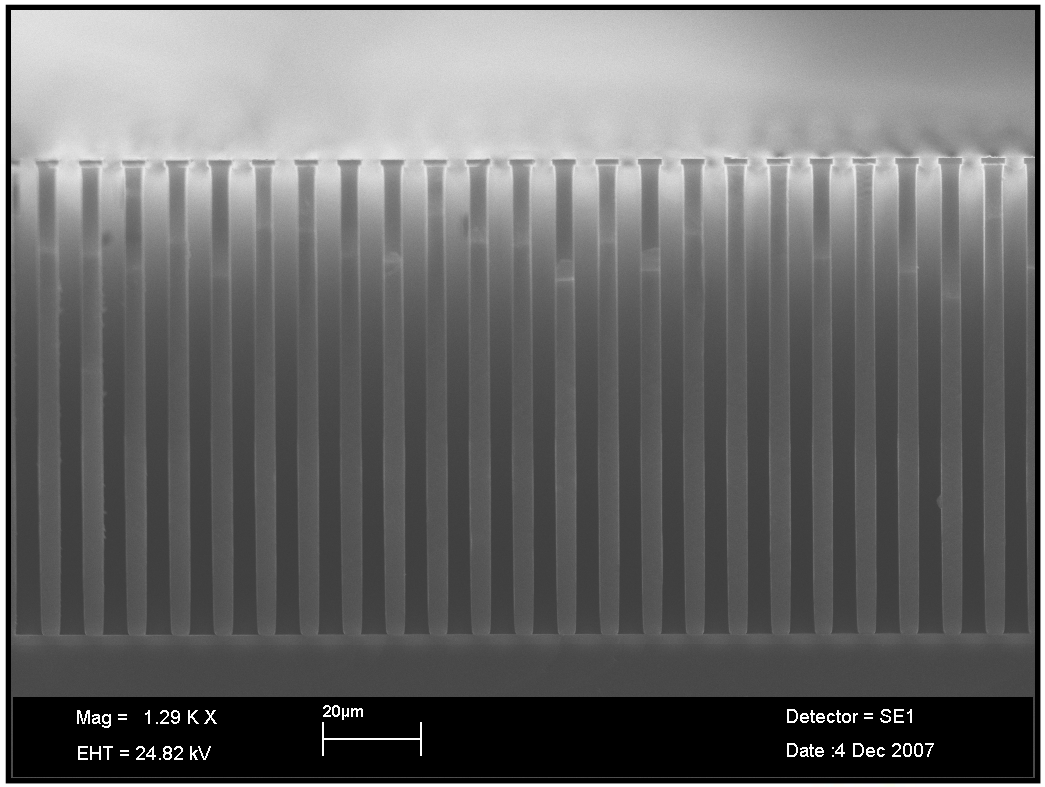
STS DRIE ASE Pegasus

Images provided by Varun Keesara & Prof. Farrokh Ayazi

Gases: SF_6, C_4F_8, O_2

STS optimized processes at the factory

3µm width: 100µm depth



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PlasmaTherm Dual DRIE SLR

Pettit Cleanroom

Dual Chamber Etching System Featuring:

- (Right) Si trench etch / poly-Si / through-wafer
- (Left) III-V etching; SiO_2 Si_3N_4 & Al / metal etching

Materials etched and acceptable masks:

- Etched/Left: SiO_2, Si_3N_4, Al, III-V → InP, InGaAs
- Mask/Left: Metal, Photoresist
- Etched/Right: Silicon, poly-Si
- Mask/Right: no metal masks (only PR, Si_3N_4, SiO_2)

Component specifications (both):

- 2000W 2.8MHz RFPP RF-20M – Coil
- 500W 13.56MHz RFPP RF-5S – Platen
- Backside Helium Cooling, both chambers
- Clamping chuck, left; electrostatic chuck, right

Gases:

- Left: Cl_2, BCl_3, C_4F_8, CF_4, H_2, Ar, O_2
- Right: SF_6, O_2, C_4F_8, Ar

Process Pressure: (5-80mTorr both chambers)

Substrate: small pieces - one 100mm wafer

Temperatures:

- Platen: Left 20°C; Right 20°C
- Chamber: 40°C

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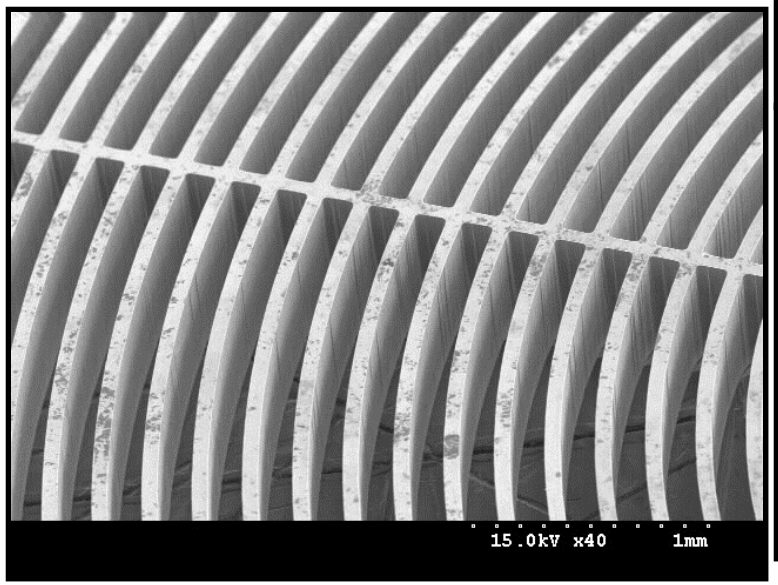
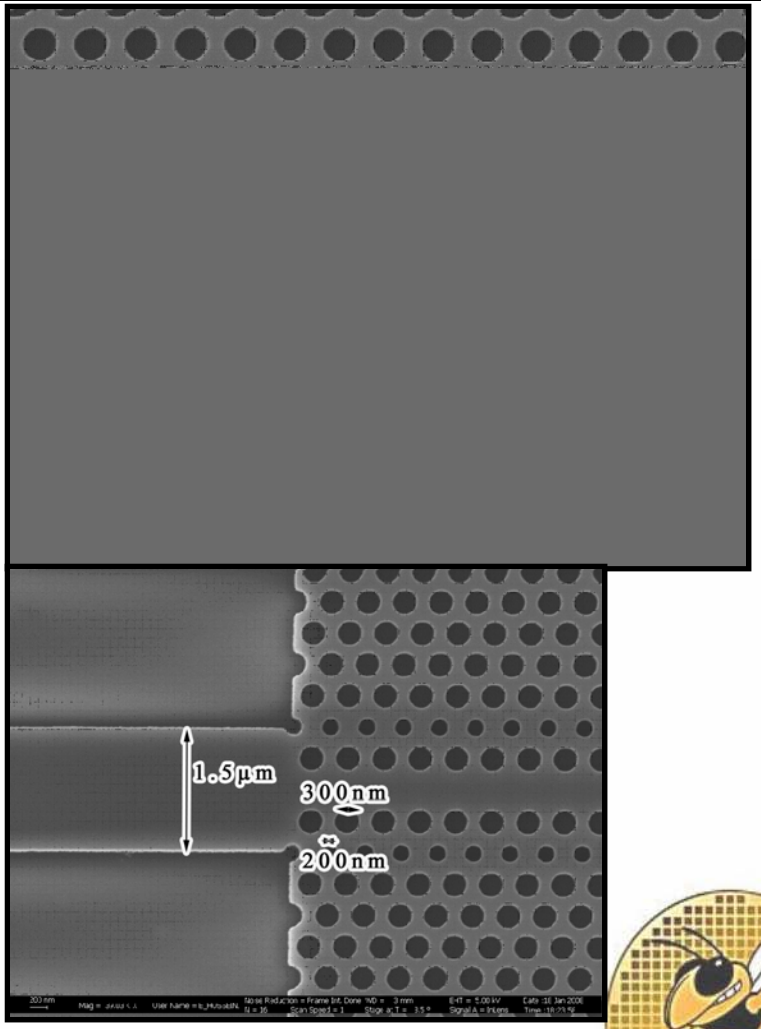
PlasmaTherm DRIE-Bosch results

Images provided by Florian Herrault. PI: Mark Allen (left) and Ehsan Hosseini. PI: Ali Adibi (right)

- **Si Trench Etch – left image:**
  - Micro-turbines
  - MEMS gyroscopes
  - MEMS accelerometers
- **Cl_2 based Si etch, right images:**
  - 2D photonic crystals
  - Waveguides





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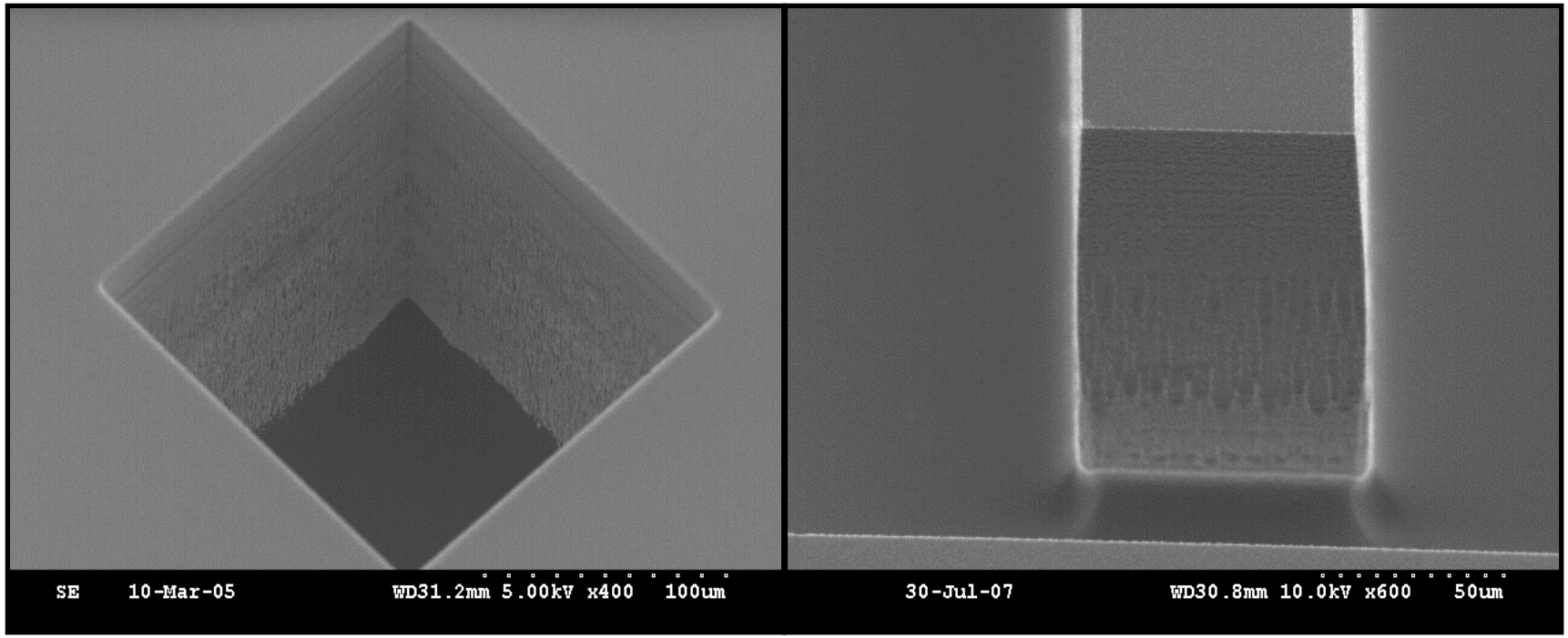
PlasmaTherm DRIE – Si Trench

Images provided by: left, Kianoush Naeli, MiRC; right, Chang-Kyeon Ji, PI: Mark Allen



Left image: through-wafer via Applications

- Through-wafer etching
- Deep trench etching for MEMS apps

Right image: cross-section of through-wafer via Rules, Right/Bosch chamber:

- No metal
- Through wafer etching requires carrier wafer

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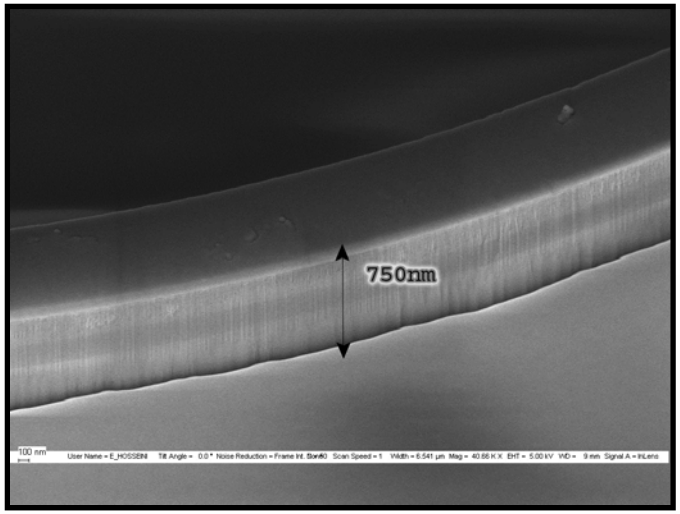
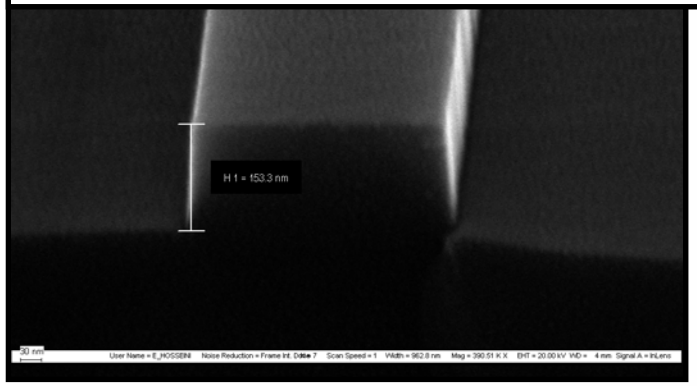
PlasmaTherm DRIE (Left) – Si_3N_4, SiO_2

Images provided by Ehsan Hosseini. PI: Ali Adibi





- Upper left: silicon nitride membrane for sensor – sensor mount rim 352.6nmSiN etch: CF_4 Resist: ZEP
- Upper right: Si-rich oxide ring – 750nm
- Lower left – silicon nitride grating bar – height 153nm

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PlasmaTherm SLR RIE

Pettit Cleanroom

RIE System Featuring:

- Loadlock and load arm

Materials etched and acceptable masks:

- Etched: Al, Cr, Ti, Si; III-V
- Masks: Photoresist; No SU8, BCB

Component specifications (both):

- 500W 13.56MHz RFPP RF-5S power supply

Gases:

- BCl_3, Cl_2, O_2, Ar, H_2

Process Pressure: 5-80mTorr

Substrate: small pieces – one 8” wafer

Temperatures:

- Platen 5-40°C

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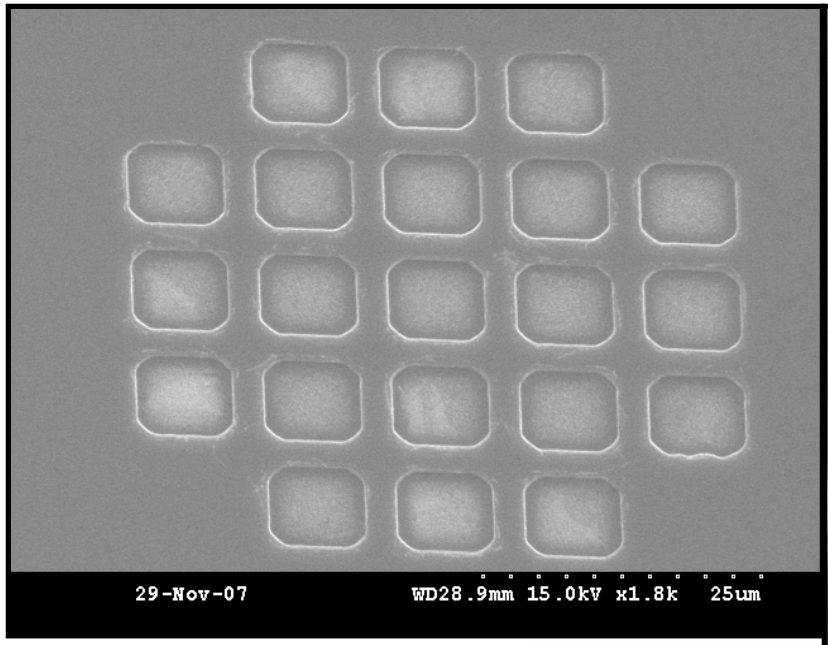
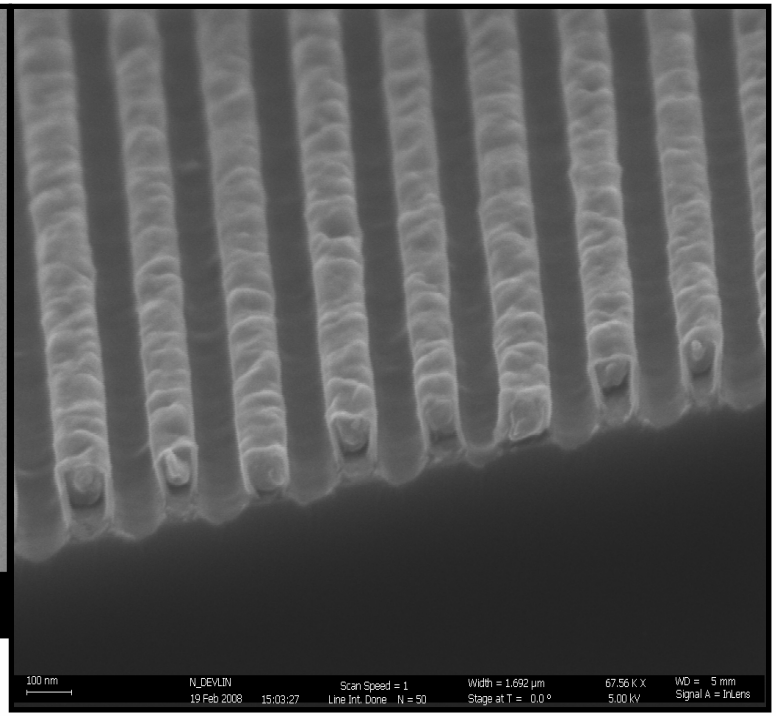
PlasmaTherm SLR RIE

Left image provided by Jiun-Hong Lai. PI: Muhanned Bakir, MiRC, ECE. Right image provided by Devin Brown & Nicole Devlin, MiRC





100nm line / 100nm space; Al on Si

Ti on Au dry etch
*ONLY Ti was exposed to plasma
Mesh 4um, **B**lock 7um, **D**iameter 50um

Pressure = 20mT
Gases: BCl_3, Cl_2 , H_2
Results: Al etch rate ~1500Ang/min

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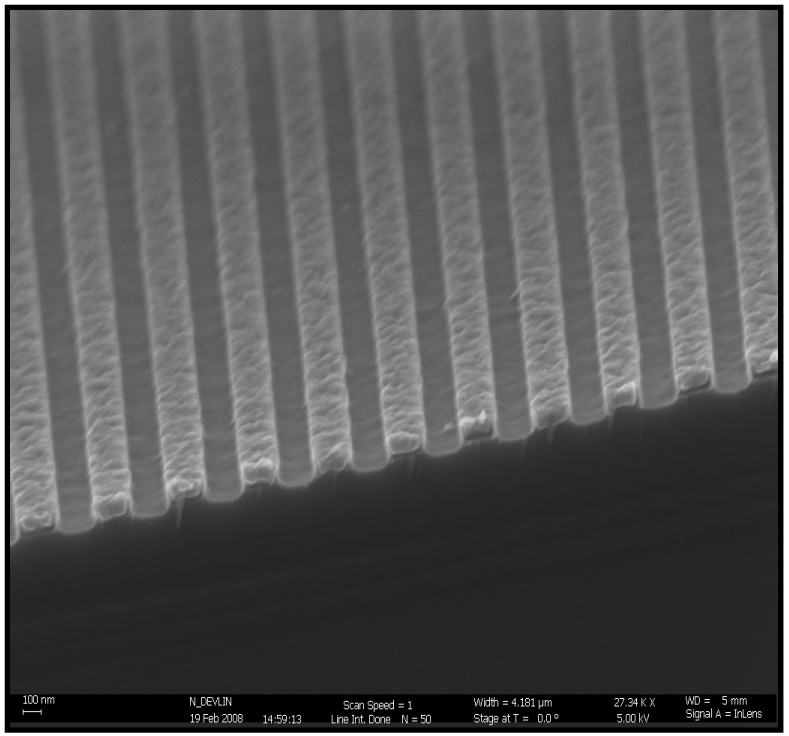
PlasmaTherm SLR RIE

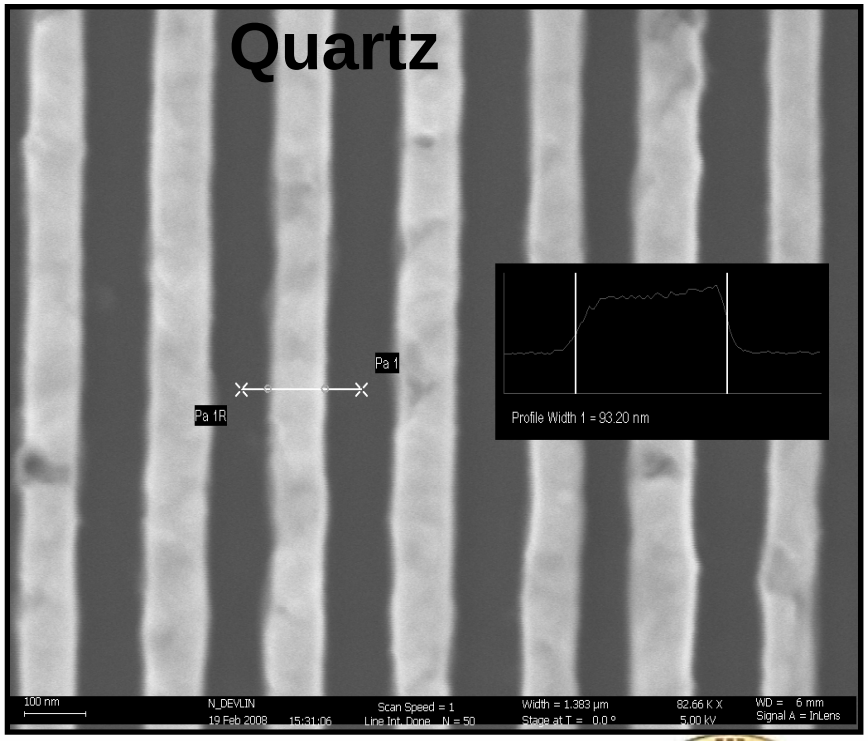
Images provided by Devin Brown and Nicole Devlin, MiRC.

Aluminum on Silicon



200nm line / 200nm space

Aluminum on Quartz



100nm line / 100nm space

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PlasmaTherm RIE

Pettit Cleanroom

Dual Chamber Etching System Featuring:

- Si, SiO_2, Si_3N_4 & Al / metal etching
- III-V etching
- Polymer etching

Materials etched and acceptable masks:

- Left: Al, Cr, Ti, Si, poly-Si, metals, III-V
- Right: Si, SiO_2, Si_xN_y polyimide, SU8. BCB
- Masks: Metal and PR

Component specifications (both):

- 500W 13.56MHz RFPP RF-5S Power supply

Gases:

- Left: O_2, BCl_3, Cl_2, Ar
- Right: Ar, CHF_3, O_2, CF_4/SF_6

Process pressure: 10-800mTorr both chambers

Substrate:

- Left – small pieces – one 8" wafer
- Right: small pieces - four 100mm wafers

Temperatures:

- Left Platen 40°C; Right 40°C

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PlasmaTherm Waf'r/Batch 790 RIE

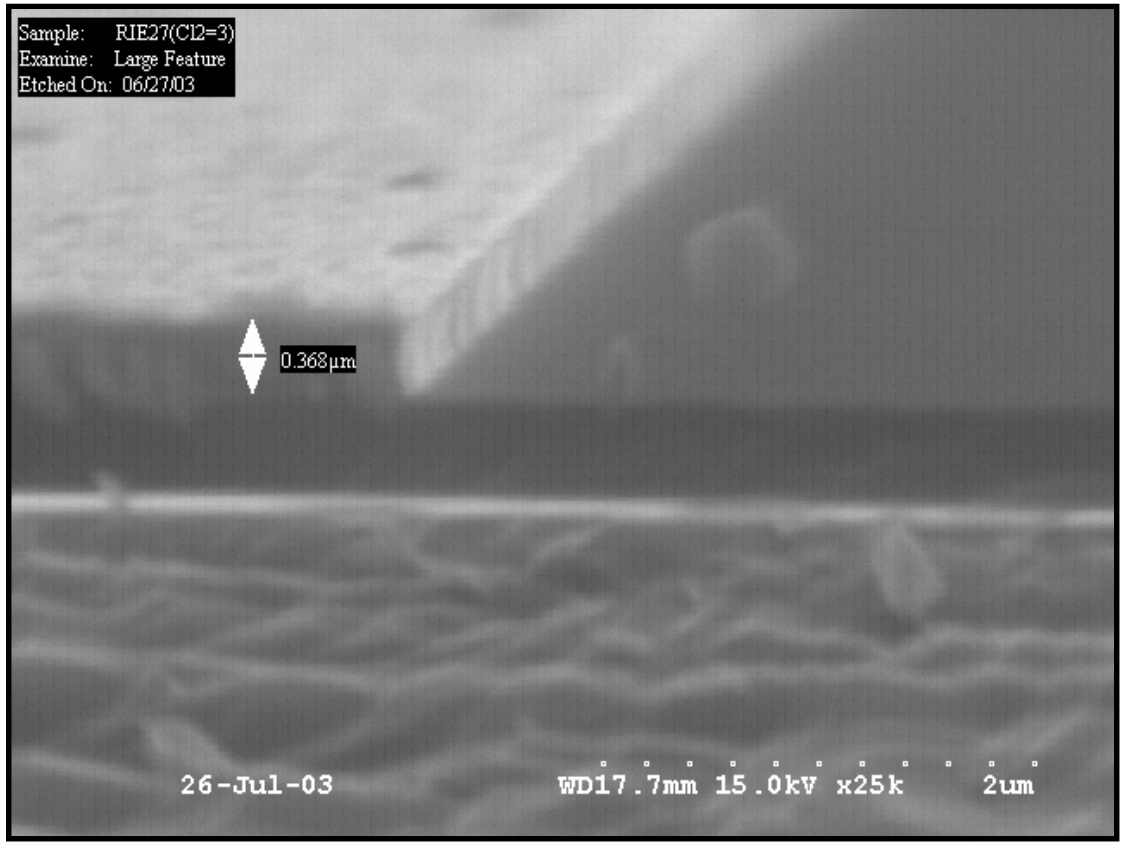
Images provided by Felicia Rainey, SURE Summer program. PI: James Zhou

Aluminum on SiO_2

- R&H S1813 resist mask
- Pressure: 40mT
- Gases:
  - BCl_3, Cl_2, $CHCl_3$

Results:

- Sidewall angle 91.15°
- No undercutting



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Advanced Vacuum Vision RIE 1

Pettit Cleanroom

RIE System Featuring:

- Third generation tool
- Vision 1 installed March 2007

Materials etched and acceptable masks:

- Etched: SiO_2, Si_3N_4, Si
- Masks: metals and photoresist

Component specifications:

- 600W 13.56MHz Seren power supply

Gases:

- Ar, N_2, O_2, CF_4, SF_6, H_2

Process Pressure: 10-800mTorr

Substrate: Small pieces – one 8” wafer

Temperature: 5-40°C

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Advanced Vacuum Vision RIE 2

Marcus Cleanroom

RIE System Featuring:

- Third generation tool
- Vision 2 installed March 2008

Materials etched and acceptable masks:

- Etched: SiO_2, Si_3N_4, Si
- Masks: metals and photoresist

Component specifications:

- 600W 13.56MHz Seren power supply

Gases:

- Ar, N_2, O_2, CF_4, SF_6, H_2

Process Pressure: 10-800mTorr

Substrate: Small pieces – one 8” wafer

Temperature: 5-40°C

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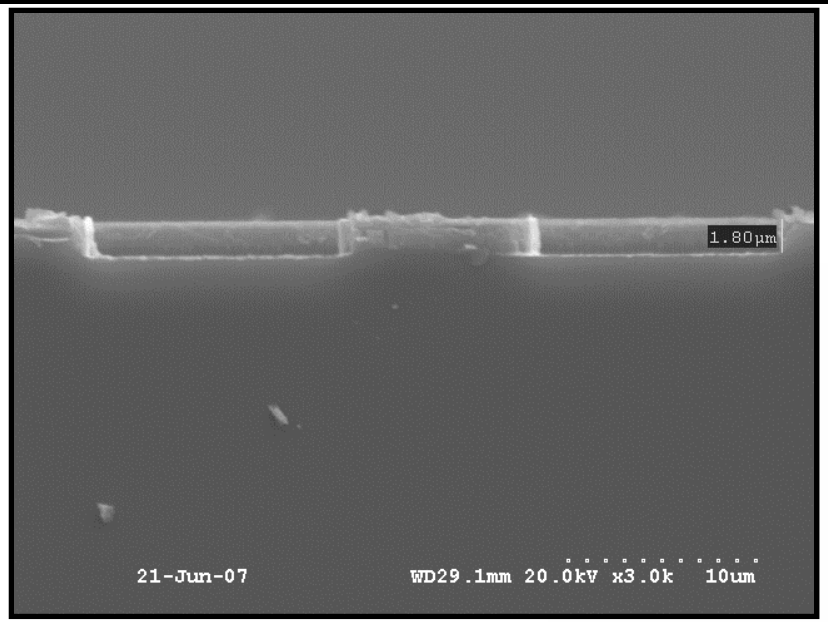
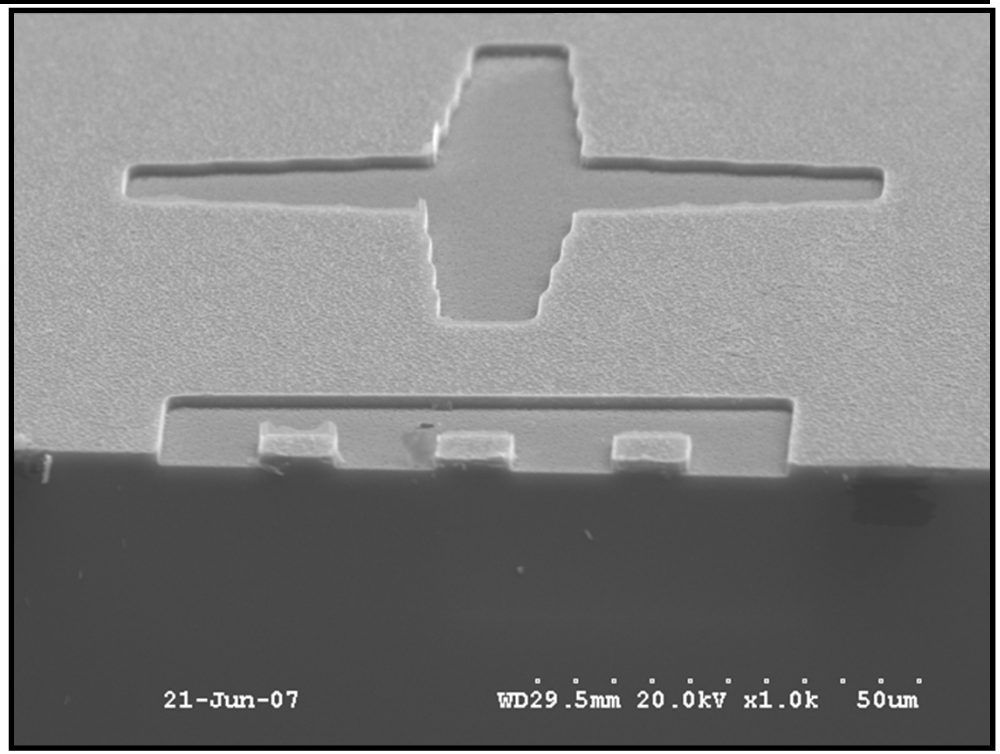
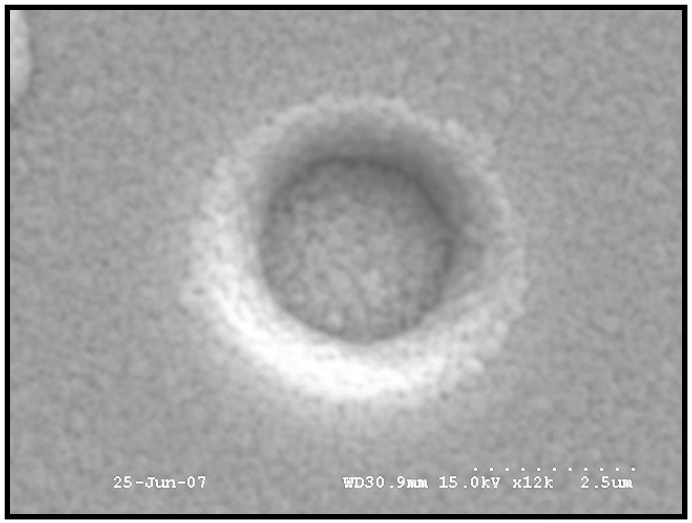
Advanced Vacuum Vision RIE 1

Lower left image provided by Jamie Zahorian. PI: Levent Degertekin, GT Dept of Mechanical Engineering. Upper left and upper right images provided by Christina Scelsi, MiRC.







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Oxford End-Point RIE

Marcus Cleanroom

Reactive Ion Etcher

Functions:

- General plasma etching

Materials etched and acceptable masks:

- Etched: SiO_2, Si_yN_x
- Masks: photoresist, metal

Component specifications:

- 500W 13.56MHz AE – Platen
- Power: 300W

Gases: Ar, O_2, CHF_3, CF_4

Process Pressure: 5-500 mTorr

Substrate: small pieces – one 4” wafer

Temperatures: 5-45˚C

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Oxford Cryogenic ICP

Marcus Cleanroom

Functions:

- Etching with wide range of temperatures

Materials etched and acceptable masks:

- Etched: Si, SiO_2, Si_xN_y, metal
- Masks: Si_3N_4, SiO_2, photoresist

Component specifications:

- 8000W 13.56MHz ENI – Coil
- 1000W 13.56MHz ENI – Platen
- Mechanical clamp

Gases: H_2, Cl_2, Ar, O_2, SF_6, He, BCl_3, CHF_3, C_4F_8, CO_2

Process Pressure: 5-80mTorr

Substrate: small pieces - one 4" wafer (smaller pieces must be mounted to a 4" wafer)

Temperatures: -150˚C-300˚C

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Unaxis RIE

Marcus Cleanroom

Reactive Ion Etcher

Functions:

- Shallow silicon etching

Materials Etched and acceptable masks:

- Si
- Masks: Si_3N_4, SiO_2, photoresist

Component specifications:

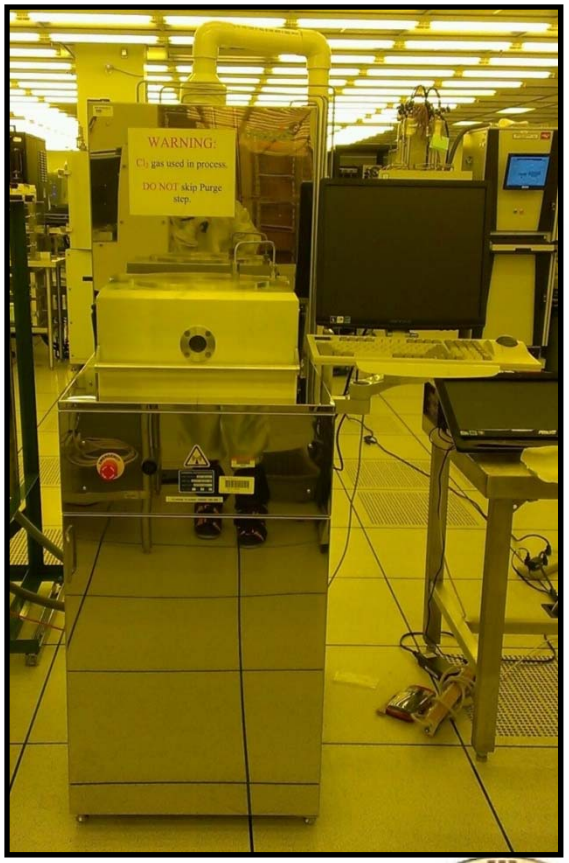
- 500W 13.56MHz AE RF5S– Platen

Gases: Cl_2,O_2, Ar

Process Pressure: 10-800mTorr

Substrate: small pieces-4” wafer (up to 3)

Temperatures: 5-40°C



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STS HRM

Marcus Cleanroom

Functions:

- MEMS-CMOS processes
- Narrow high aspect-ratio trench etching

Materials etched:

- Etched: Si, SOI wafers

Masks:

- SiO_2, Si_xN_y
- Photoresists: SC1800 series, SPR220 from Shipley, AZ4000 series from Clariant, NPR from Futurex

Component specifications:

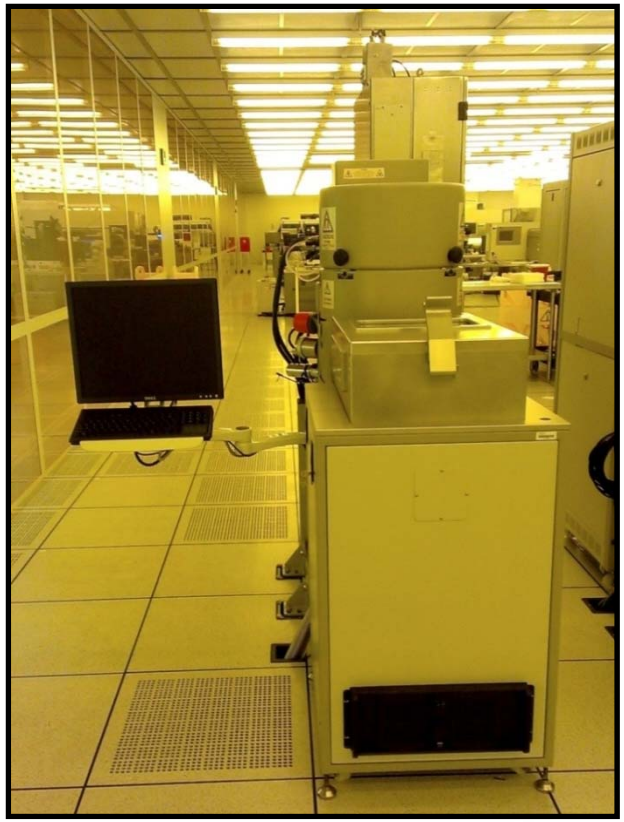
- 3000W 13.56MHz AE – Coil
- 500W 13.56MHz ENI – Platen
- 500W 380KHz AE LF5 – Platen
- Backside helium cooling with electrostatic chuck

Gases: SF_6, C_4F_8, Ar, O_2, CO_2

Process Pressure: 5-80mTorr

Substrate: small pieces (with carrier wafer) - 6” wafers

Temperatures: -20˚C-100˚C



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Y.E.S.-R1 Plasma Cleaner

Pettit Cleanroom

Functions:

- Descum and remove residual organics and thin oxides

Component specifications:

Gases: O_2 , Ar, N_2

Process Pressure: 1500mTorr

Substrate: size varies upon user request

Temperatures: 25-80˚C

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Gasonics Asher

Marcus Cleanroom

Functions:

- Photoresist stripper for front and backsides of wafers
- Descummer (200-500 Angstroms of photoresist)
- Remove max 1 micron each run

Component specifications:

- Load arm

Gases: O_2 and N_2

Process Pressure:

Substrate: 4” wafers, 1-10 wafers per run

Temperatures: 25-200°C

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Xactix XeF_2 e1 Series Xetch

Marcus Cleanroom

Vendor-specified system features:

- Excellent selectivity SiO_2:Si (1000:1), good selectivity to PR
- Potential to etch very small devices (30nm)
- Etch does not attack Bosch passivation layer – can switch between tools and still protect trench walls

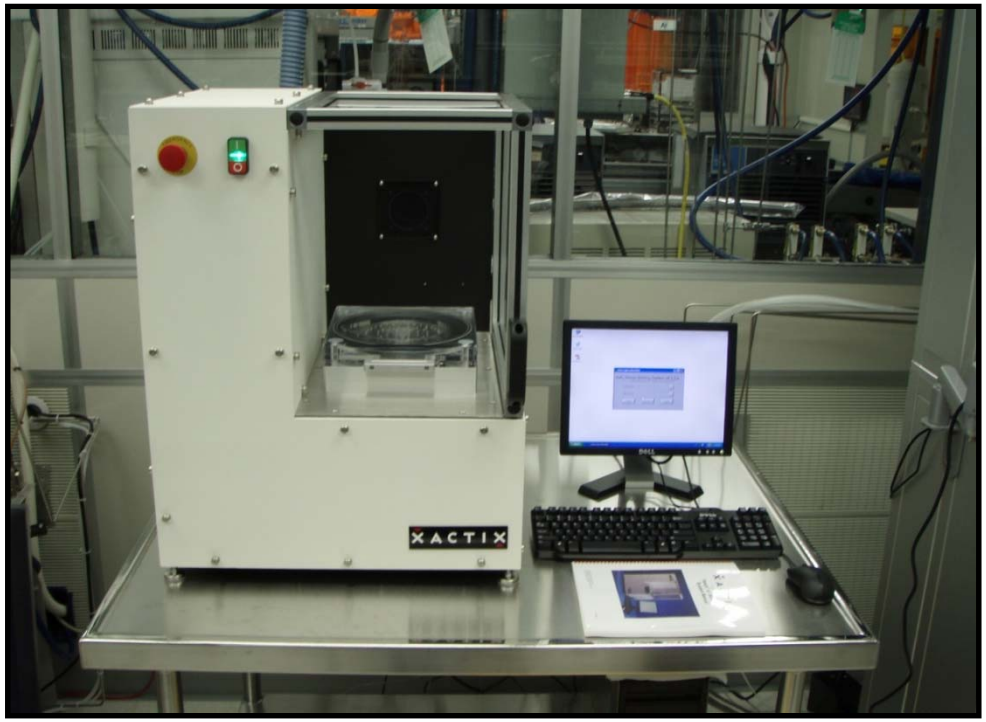
Tool currently being qualified – install just completed

Materials etched and acceptable masks:

- Etched: Si, poly-Si
- Masks: PR, SiO_2, Si_3N_4

Gases: XeF_2

Substrate: 1 die - 150mm wafer (specialized chuck)



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Baseline Testing

Setup test protocols

- Substrate standard
  - 4 in Silicon wafer with 100 orientation
- Preparation of etching mask
  - SPR220.7, 7.5um, hard baked for 40 min @ 100C in oven
- Etching pattern
  - Trenches vs. TSVs
- Test result
  - Uniformity, etch rate, etch profile, selectivity

Collecting baseline data periodically

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Developing New Application

Etching dielectrics on STS HRM

- Electro-static chuck
  - More efficient transfer
  - Less time needed for sample preparation
- CO_2 gas
  - Allowing for dielectric etching
- Greater advantage in higher selectivity
  - Photoresist vs. dielectric materials

Etching Si on Oxford Cryogenic ICP

- pseudo-Bosch silicon etch
  - Advantages:
    - Smoother sidewall compared to conventional Bosch process (straight etch)
    - Higher selectivity
  - Disadvantage:
    - Only for trenches, lines, and boxes

High frequency recipe on STS Pegasus

- Working with SPTS process engineers to develop high frequency recipe
  - All current recipes are low frequency recipes

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Setup Online Process Library

Standard recipe collection

- Monthly baseline tests of standard recipes
- Characterization of results: etch rate, uniformity, selectivity

Standard operation procedure

- Compile all standard procedures into one database
- Similar machine procedures are grouped together

Equipment configuration

- Differentiation between RIE and ICP tools

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Maintenance Strategies

Reactive Maintenance

- Schedule maintenance around user request
- Run-to-failure

Predictive Preventative Maintenance

- Use periodic baseline testing to predict when a tool will need maintenance.
- Monitor facilities to predict when pumps, chillers, and other relevant hardware will need service.

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Acquisitions & Upgrades

No future acquisitions planned

Future upgrades

- Many of our future equipment upgrades will be performed in-house
- Custom software using existing hardware using Allen-Bradley PLC supported by Rockwell Automation software.

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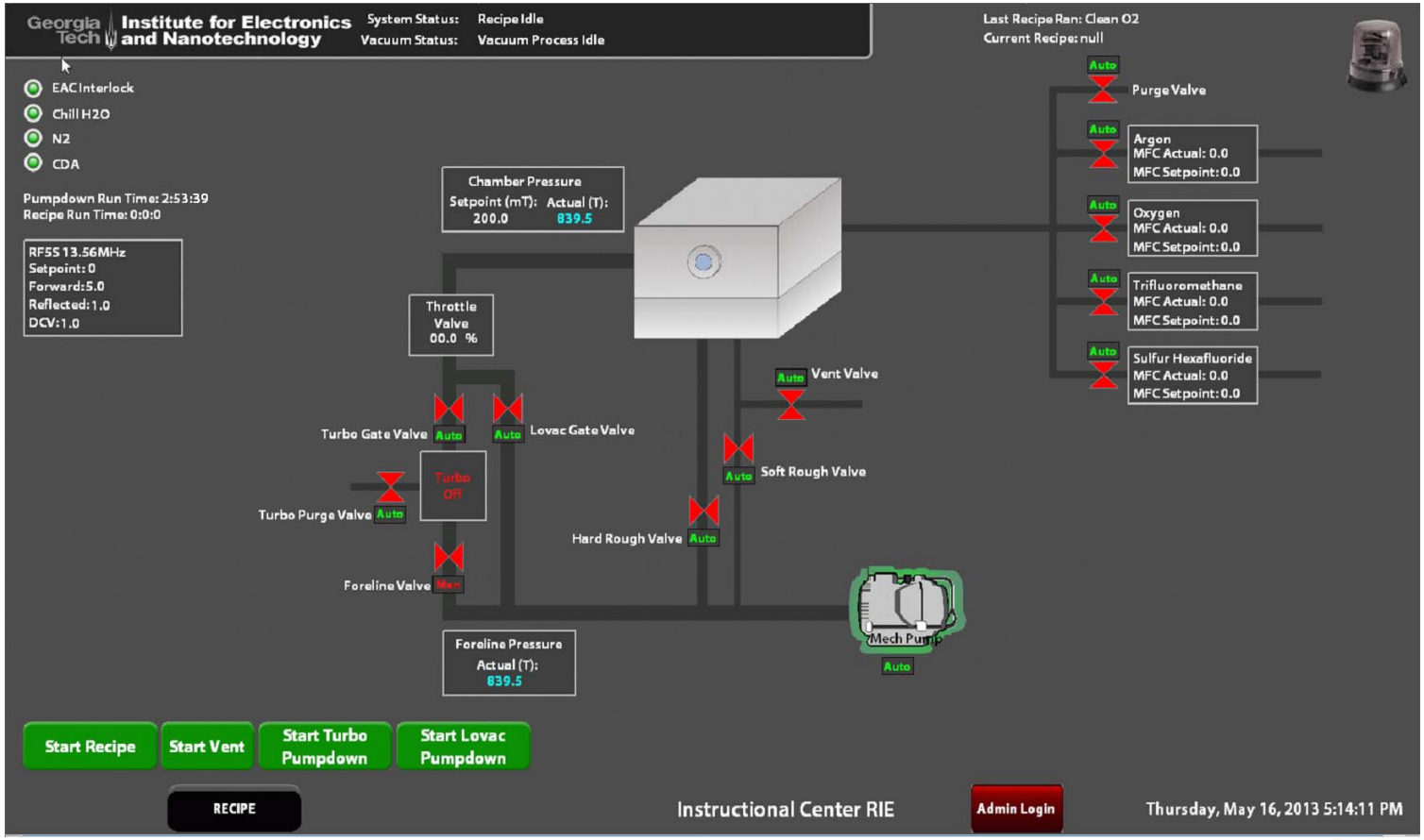
Acquisitions & Upgrades



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QUESTIONS?

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